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Enhancing Signal Integrity in GPS-Focused PCB Designs: A Comprehensive Approach

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Abstract

Electromagnetic interference (EMI), Signal Integrity (SI), and power delivery represent critical challenges in the design of high-density interconnect Printed Circuit Boards (PCBs). Performance degradation due to parasitic effects, impedance discontinuities, and crosstalk often results in electromagnetic compatibility (EMC) violations. This paper proposes a comprehensive design methodology based on optimized layer stack-up, controlled impedance routing, and strategic via placement to enhance EMC compliance and SI in compact, high-performance PCBs, with a particular focus on GPS applications operating at 1.575 GHz. These design strategies support the implementation of 50-ohm controlled microstrip lines, well-defined ground planes, and robust power distribution networks. Using simulation tools such as MATLAB, CST Studio Suite, and Altium Designer in conjunction with transmission line theory, key performance metrics, including return loss, voltage standing wave ratio (VSWR), and insertion loss, are assessed. The proposed design is implemented on a custom GPS PCB and empirically evaluated using Teseo Suite, confirming enhanced spatial efficiency, reduced reflection, and improved GPS signal acquisition and tracking. Research findings highlight the efficacy of simulation-driven PCB design practices in addressing high-frequency signal degradation and EMI concerns, with broad applicability to automotive, telecommunications, and consumer electronics domains requiring reliable GNSS functionality. The integration of GPS technology into everyday electronics, such as smartphones and autonomous vehicles, highlights the increasing demand for efficient and reliable signal integrity. The continuous demand for faster, smaller, and more affordable electronic devices underscores the rapid evolution of PCB technology and the necessity for strict design policies, especially in Gigahertz (GHz) systems. This work concludes by validating the proposed design methodology through a compact GPS-PCB model, demonstrating improvements in signal integrity and spatial efficiency.

Keywords: *Altium Designer, CST Studio Suite, Electromagnetic Interference (EMI), GPS, PCB.*

1. Introduction

With the advent of highly integrated electronic technologies, fabrication marks a convergence with interconnect traces and component packaging, giving rise to Ultra-High-Density Interconnect (PCBs). Although small feature sizes improve performance and capabilities, new challenges should be addressed, particularly in maintaining signal integrity (SI), managing electromagnetic interference (EMI), and ensuring reliable power delivery. These challenges are further intensified by the rising operational frequencies of modern devices, where higher speeds make systems more vulnerable to parasitic effects and signal degradation. As data rates and transmission speeds grow, PCB design has become significantly more complex. Today's

high-speed digital systems require precise impedance control, effective EMI mitigation, and carefully designed power distribution networks to meet strict electromagnetic compatibility (EMC) standards. Managing signal and power paths with precision has become essential, especially as interconnects increasingly behave like transmission lines at these frequencies [1].

Operating in the GHz frequency range tends to cause problems such as signal losses, attenuation, and power dissipation during transmission, which cause a degradation of system performance and reliability [2]. Furthermore, at high frequencies, SI is susceptible to impedance mismatches at circuit connections, such as device connection pins, vias, and PCB trace discontinuities, particularly when the electrical wavelength is shorter than the trace length [3], [4], therefore, a precise impedance matching should be done to preserve signal integrity and prevent distortion. In high-speed PCB design, impedance control is performed by the correct trace spacing, trace width modifications, and layer stack-up distribution using predefined dielectric constant materials. Careful selection of routing guidelines, together with EMI shielding, all contribute to overall PCB performance and enable high-speed data transmission [5], [6]. Transmission lines are prone to high-frequency effects, including reflection and attenuation, which significantly reduce the quality of the signal at high data speed digital systems. The trace on a printed circuit board (PCB) may be thought of as a perfect channel at the direct current (DC) operating point since it is free of capacitance, inductance, and resistance. Analog circuit features, however, predominate at higher frequencies. As a result, the channel is significantly impacted by parasitic resistance, inductance, and capacitance. A simple circuit model can be used to depict the trace on a PCB. These parasitic components determine the characteristic impedance of the PCB trace. Signal quality deteriorates with any impedance discontinuity or mismatch along the transmission channel. The uneven impedance of the transmission line, receiver's input, and transmitter's output results in the impedance mismatch. As a result, the leftover energy is reflected to the transmitting end, leaving the broadcast signal to only partially reach the receiver. Because of the reflection, the signal is weakened or warped. The receiver's ability to accurately interpret data is impacted by the degree of signal attenuation. When there is severe signal distortion, the receiver may misinterpret the data, resulting in data error [7].

Electromagnetic Interference EMI, defined as the unwanted disturbance caused by electromagnetic energy, arises when EMC compliance is violated. Since 1996, adherence to EMC regulations has been mandated across the European Union, requiring all electrical and electronic devices to neither emit harmful electromagnetic radiation nor be adversely affected by such emissions from external sources. Compliance with these standards has thus become a critical objective in PCB design, especially for high-speed, high-frequency applications. Several researchers have proposed methodologies to address these growing challenges. Yildiz and Coskun [1] provided a comprehensive framework for designing PCBs with reduced EMI and enhanced EMC by combining experimental observations, theoretical models, and practical engineering techniques. Degerstrom, Smutzer, Gilbert, and Daniel [2] analyzed PCB architectures capable of supporting 56 Gbps NRZ signaling, emphasizing the role of insertion loss, skew, and signal integrity, while investigating via stubs, pin-field breakouts, and fiber weave skew through simulations and measurements. Li [3] introduced a low-loss hybrid-plane PCB design to reduce material costs and enhance signal quality using reduced amounts of PTFE. In a related effort, Singh, Anand, and Ladwal [4] examined common PCB design errors and proposed strategies for optimizing power converter layouts. They provide sufficient signal integrity, maximize thermal management, lower parasitic inductance, and enhance component placement by using trace width calculations and high-voltage isolation techniques. The book functions as a reference manual for high-speed PCB layout. In [8] a low-loss hybrid-plane PCB layout has been developed to enhance signal quality in high-speed transmission lines and reduce the cost of low-loss dielectric materials. This design uses less PTFE and achieves similar signal quality benefits as conventional hybrid PCBs, resulting in significant cost savings. The low-loss dielectric layer should be at least 80µm thick. Thongrattana and Manoppong [9] applied a Design of Experiment (DOE) methodology to optimize parameters in a surface-mount technology (SMT) process for flexible printed circuit boards (PCBs). To decrease errors in the solder printing process, it focuses on correcting variations in solder volume. The researchers discovered that solder volume uniformity is greatly impacted by print speed, print pressure, print range, and clearance. They identified ideal parameter levels for reducing waste and reaching almost 100% solder volume on target. Rayas-Sánchez et al. [10] The paper proposes a method to enhance signal and power integrity and power delivery networks in high-speed links using surrogate-based optimization, focusing on space mapping techniques, and presents a computationally efficient parameter extraction methodology. The techniques for measuring and lowering electromagnetic interference (EMI), such as GTEM cells, RCs, OATS, and LSNs, are thoroughly examined in [11]. It also covers electromagnetic shielding, EMI reduction strategies, and EMI emission and immunity testing methods. Additionally, the writers investigate EMI filters, circuit topology modifications, and spread spectrum. Practical aspects of EMI measurement and control, including testing procedures and real-world application difficulties, are also included in the paper. The study in [12] explored recent advancements in flexible electromagnetic interference shielding material design, focusing on enhancing green shielding performance by balancing reflection and absorption loss, using inherently flexible materials like graphene foams and aerogels.

Additional progress in the field includes the work of Yasunaga et al. [13], who developed a Capacitor Segmental Transmission Line (C-STL) structure. By applying genetic algorithms, they optimized the placement and values of embedded capacitors to enhance signal integrity in high-speed circuits. Menićanin et al. [14] used vector network analyzer testing to extract critical parameters of ferrite-based EMI suppressors, improving their accuracy for practical PCB applications. Berzoy et al. [15] also applied genetic algorithms in combination with 3D finite element methods to optimize magnetic field distribution and reduce EMI in power converters. In a more data-driven approach, Ecik et al. [16] proposed a decision tree–

based AI technique to detect signal integrity issues in transmission lines, showcasing its promise as a predictive diagnostic tool for complex electronic systems. A detailed review of EMI modeling techniques for automotive integrated circuits (ICs), analyzing commonly used models such as IBIS, ICEM, and IMIC, was provided by Baba et al. [17]. EMI mitigation approaches and measurement techniques relevant to modern automotive electronics were examined by studying the shielding strategies. Lastly, Timsit [18] addressed the challenges in designing high-frequency connectors, offering practical insights into improving impedance matching, minimizing insertion loss, and reducing crosstalk. His recommendations covered waveguide structures, dielectric material selection, and the use of back-drilling for optimal connector performance.

This work aims to develop and validate a design methodology for PCBs with enhanced signal integrity, focusing specifically on GPS-enabled systems. The main objectives are: (1) to describe the effects of the main design elements such as trace geometry, architecture, and dielectric material properties. (2) implement a systematic PCB layout optimization process encompassing signal routing, layer stack-up, and power distribution network (PDN) design; and (3) evaluate the proposed methodology using computational electromagnetic (CEM) simulations to measure improvements in SI performance metrics such as Reflection Coefficient, Crosstalk, and Return Loss (RL). Guidelines for component location, signal routing, layer stack-up design, and PDN design are provided by this methodology.

2. Methodology

In this section, the design approach used to develop a high-performance PCB tailored for GPS operation at 1.575 GHz is described. The aim was to ensure strong signal integrity, effective electromagnetic compatibility (EMC), and stable power delivery in a compact and efficient design manner. Several key elements were considered in this methodology: integrating various communication interfaces with designing an optimized layer stack-up, fine-tuning trace geometry and spacing to achieve smooth system connectivity.

2.1 PCB Stack-Up Design

To balance signal integrity, EMI suppression, and a guaranteed return path, a four-layer PCB design was selected. This approach offers strong support for Gigahertz signal transmission while maintaining high SI and reducing EMI. Each layer in the stack-up was carefully arranged to suppress noise coupling, enhance overall electrical performance and provide clear return paths for signals, as follows:

- **Top Layer (Signal 1):**
  The main signal paths and the GPS antenna feed (Gigahertz signals) are routed in this layer. To obtain a reduction in transmission losses and signal reflections, 50-ohm controlled microstrip lines were used.
- **Second Layer (Ground Plane 1):**
  A low impedance return path for high-speed and RF signals is provided through a solid, uninterrupted ground plane. Moreover, it also serves as an effective shield, helping to reduce crosstalk and suppress electromagnetic interference (EMI).
- **Third Layer (Ground Plane 2 / Power Plane):**
  Sensitive RF traces are isolated from digital signals using this layer, acting either as an additional ground or power layer. Additionally, it also contributes to EMI control and supports stable power distribution, especially in circuits with higher current demands.
- **Bottom Layer (Signal 2):**
  The low-speed digital signals, like UART and I²C are routed in this layer by offloading these signals from the top layer, reducing congestion and minimizing the risk of interference with RF paths.

Adopting this stack-up strikes a balance between compact size, manufacturing feasibility, and excellent electromagnetic performance.

2.2 Trace Geometry and Impedance Matching

Different trace-level optimizations are tested to meet the Gigahertz performance requirements of the GPS:

1. **Controlled Impedance Traces:**

The microstrip impedance was designed as 50-ohm for all RF traces. The calculations were performed using MATLAB, using the following stack-up values, see Figure 1:

- Substrate: FR-408HR 2113
- Dielectric thickness: 0.199898 mm
- Top copper thickness: 0.0432054 mm
- Ground plane thickness: 0.0175006 mm
- Trace width: 0.3971798 mm

2. **Trace Spacing:**

The "3W rule" method was applied to prevent capacitive and inductive coupling. In which the trace spacing requires adjacent lines to be spaced at least three times their width apart. Additionally, Gigahertz and RF traces were physically separated to minimize mutual interference [2], [6].

3. **Length Matching for Differential Pairs:**
   D+ and D−, the differential signal pairs of the USB, are kept with the same length and routed with a controlled impedance of 90 ohms to prevent timing skew and obtain high-speed signal integrity [3].

4. **Avoidance of Sharp Angles:**

All trace corners were bent using 45-degree angles instead of sharp right-angle turns to keep consistent impedance and reduce signal reflections. This approach enables smoother signal propagation for Gigahertz GPS signals [4].

2.3 Communication Interface Integration

To achieve flexible and effective communication with other systems, several common protocols are integrated in this design, including:

- USB
- UART (via FTDI chip)
- I²C

The sensitive RF signals on the top layer should be isolated; therefore, these lines were routed on the bottom signal layer, with careful spacing and isolation techniques implemented.

2.4 Power Delivery Network (PDN) Design

To maintain clean and stable power delivery while suppressing coupling between power lines and RF signals, a robust PDN is performed:

1. **Power/Ground Plane Coupling:**
   Planar capacitance was improved by the proximity of the ground and power planes, which reduced high-frequency noise and provided more decoupling. [2]. To maintain low impedance when the first layer was utilized as a signal plane, it was closely connected with nearby ground planes [3].
2. **Ground Stitching:**
   The ground planes were connected by carefully positioned vias, which decreased ground loop inductance and contained electromagnetic interference [4].
3. **PDN Impedance Analysis:**
   Altium Designer was used to model and adjust the PDN impedance, guaranteeing steady voltage levels and reducing noise throughout the working frequency range. [5]. These PDN techniques preserved the integrity of high-frequency transmissions while guaranteeing dependable power delivery.

These PDN techniques contributed significantly to maintaining the integrity of high-frequency signals and ensuring reliable overall system performance.

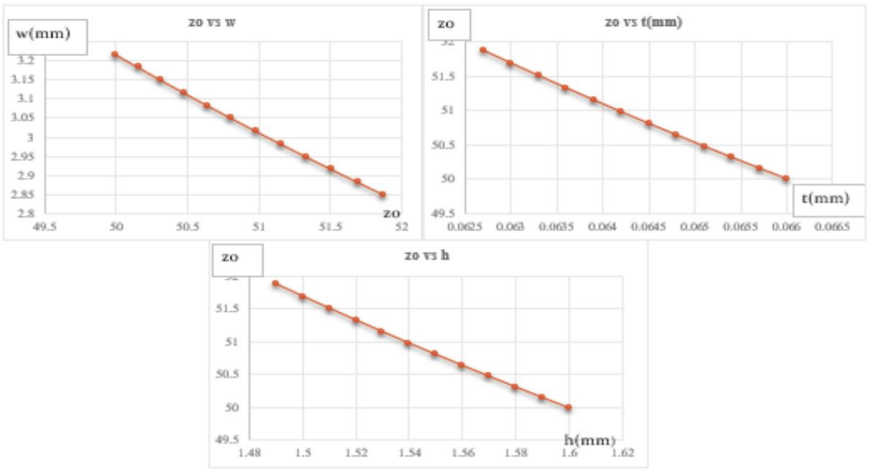

FIGURE 1. The relationship of trace thickness and trace width is inverse, and that's because increasing these factors increases the amount of current passing in the Microstrip, while increasing the height of DK makes the impedance increase

3. Signal Integrity Analysis

The signal integrity analysis for the GPS-focused PCB design, running at 1.575 GHz, was performed using the CST Studio Suite, a robust simulation tool for analyzing electromagnetic behavior.

3.1 Simulation Setup

The analysis was performed using the frequency-domain solver in CST Studio Suite to accurately model the PCB's high-frequency characteristics. Below are the key simulation parameters included:

- **Frequency Range:** 1 GHz to 2 GHz, with a primary focus on the operational frequency of 1.575 GHz
- **Mesh Type:** Hexahedral mesh, providing high resolution and numerical accuracy
- **Mesh Cells:** 136,242 cells, enabling detailed modeling of critical geometries
- **Boundary Conditions:** Open (add space) boundaries were applied in all directions to simulate a realistic electromagnetic environment
- **Excitation Method:** Waveguide ports were used to define input/output interfaces for signal injection and analysis

3.2 Results and Validation

Simulation results indicated that the transmission lines maintained a consistent impedance, matching the design target of 50 ohms. Notably, the Voltage Standing Wave Ratio (VSWR) at 1.575 GHz was found to be close to 1, confirming excellent impedance matching and minimal signal reflection. These simulation insights were instrumental in refining the transmission line geometries during the PCB layout phase. The validated transmission line design was implemented consistently across all manufactured boards using Altium Designer. The CST simulation data, including impedance plots and VSWR curves (see Figure 2), confirmed the signal quality and validated the effectiveness of the PCB design strategy.

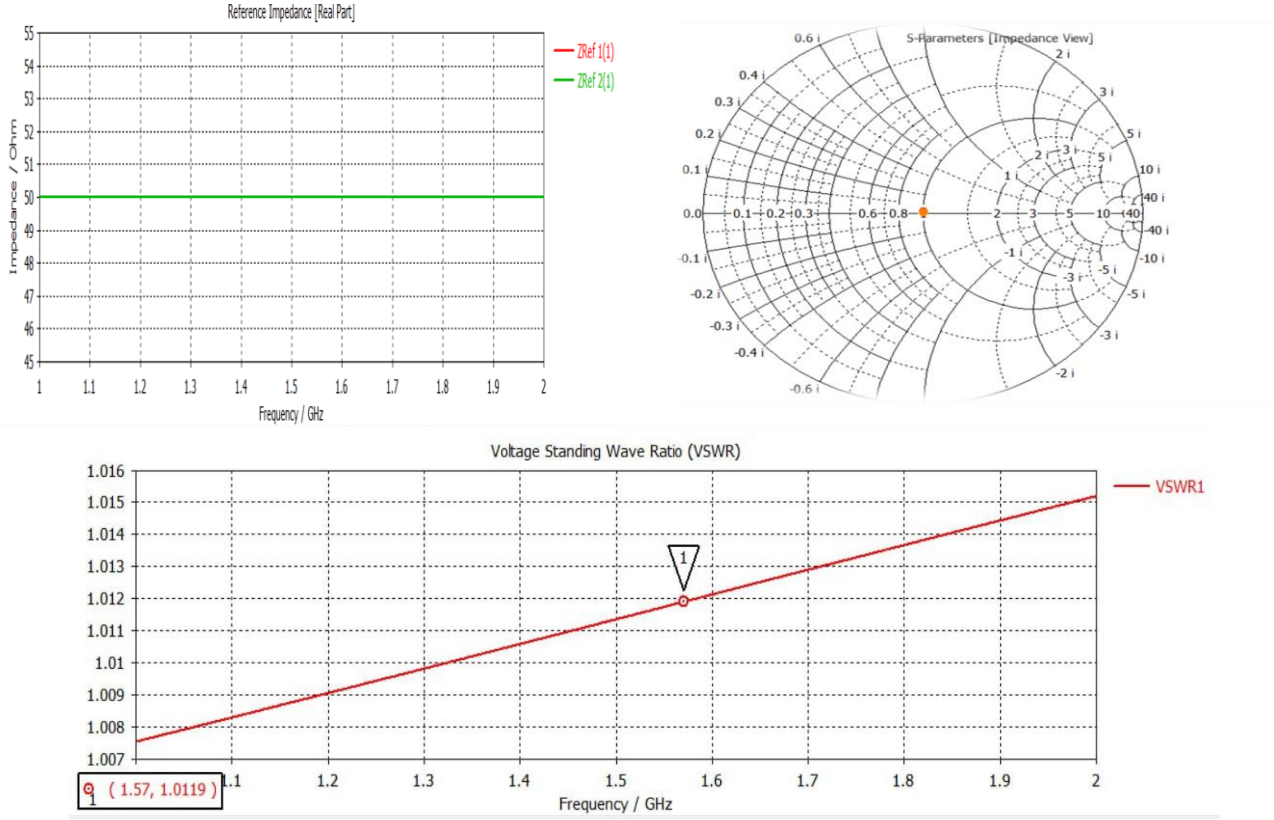

FIGURE 2. Results from CST Studio show the accuracy of the impedance calculation and also a VSWR value with the Smith chart explain

3.3 CST Studio Suite Simulations

To analyze and optimize the high-frequency behavior of the PCB, simulations were conducted using **CST Studio Suite**, a powerful electromagnetic field solver. Special attention was given to critical metrics such as:

- Characteristic Impedance
- Insertion Loss
- Return Loss

The RF traces were designed as 50-ohm microstrip lines to ensure efficient power transfer and minimize signal reflections. Simulation results showed a consistent impedance along the entire RF path with low insertion loss, confirming that the trace geometry and PCB layer stack-up were well-optimized. These CST-based simulations were essential in desibning the final PCB layout. The optimized transmission line design was applied equally across all PCB traces. This maintained high signal integrity and reliable performance, especially in the GPS antenna path, where preserving RF signal quality is critical. The simulations confirmed a continuous 50-ohm impedance from the GPS antenna through the Low Noise Amplifier (LNA+) and into the subsequent RF stages. 50 50-ohm impedance match greatly reduced signal reflections and improved RF power transfer, both of which are key to achieving an accurate and stable GPS signal.

3.4 Integration with PCB Layout in Altium Designer

In the previous section, the transmission line design was validated using CST Studio Suite. Now, the final PCB implementation needs to be completed using Altium Designer to achieve precise control over the important trace parameters like length, width, spacing, and layer assignment. This allows the physical design to closely reflect the simulation results. This accurate implementation of the simulated RF design into the physical layout using Altium ensures strong signal integrity across the device, which is crucial for reliable GPS operation at the target frequency of 1.575 GHz. Figure 3 illustrates the 2D cross-section of the trace routing, showing how trace geometry, layer usage, and spacing techniques were all aligned with the simulation-driven approach, confirming a smooth transition from design to application.

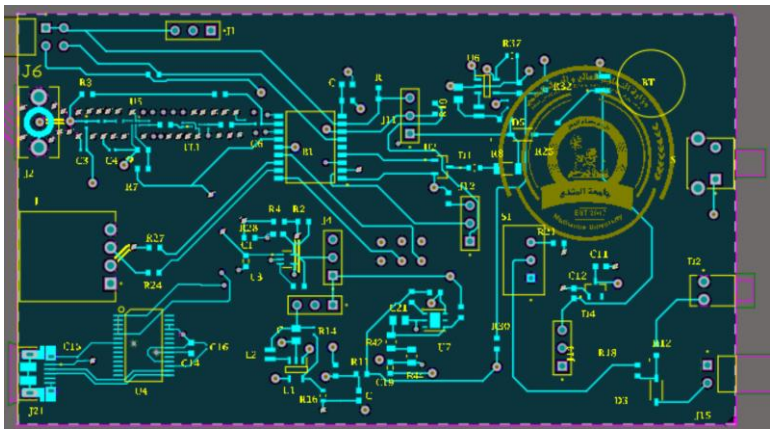

FIGURE 3. 2D cross-section illustrating trace routing strategies

4. GPS Module Integration

Achieving reliable GPS performance, the Teseo-LIV3F GNSS module was inserted into the PCB. This process followed established RF design principles, layout constraints, and communication protocol requirements to optimize overall system performance. Key design considerations included strategic antenna placement, clean and direct RF signal routing, effective noise isolation, and robust communication interface implementation.

4.1 Optimal Component Placement

- **Antenna Placement:**
  GPS antenna [on top] layer of the PCB to avoid noisy digital parts, and power traces for best satellite signal reception by the GPS antenna. EMI was decreased and a visible line-of-sight reception was provided.
- **Ground Plane Beneath Antenna:**
  A continuous ground plane was right beneath the antenna and feed line, which supplies a golden return current path and improves the signal-to-noise ratio. It also served as a buffer to attenuate external noise sources into the GPS signal.

4.2 RF Path Design

To preserve signal integrity and minimize losses from the antenna to the GNSS module, the RF path was carefully designed with the following principles:

- **Controlled Impedance:**
  The RF trace connecting the antenna to the Teseo-LIV3F module was designed as a 50-ohm microstrip line, reducing signal reflections and improving RF power transfer.
- **Short and Direct Routing:**
  RF traces were kept as short and direct as possible to minimize insertion loss and parasitic effects. Minimal via transitions were used, and when necessary, via placement was optimized to maintain impedance continuity.
- **Signal Conditioning:**
  A Low Noise Amplifier (LNA) was placed close to the antenna to amplify weak GPS signals and minimize noise. An L1 bandpass filter was added after the LNA to suppress out-of-band noise and allow only the 1.575 GHz GPS frequency to pass through.
- **Trace Isolation:**

RF traces were routed away from digital signal lines and power traces to minimize coupling. Ground vias were used to isolate and shield sensitive traces from surrounding interference sources.

4.3 Communication Protocol Integration

The Teseo-LIV3F module supports multiple communication interfaces, enabling flexible system integration:

- **UART Interface:**
  The module's UART output was connected to the microcontroller for GNSS data exchange. An FTDI chip was used to convert UART signals to USB, enabling external communication with computers. Proper separation was maintained between UART and RF traces, and decoupling capacitors were placed near the FTDI's power pins to suppress switching noise.
- **I²C Interface:**
  Peripheral devices such as configuration tools or sensors were connected via the I²C bus. Pull-up resistors were included on the SDA and SCL lines to maintain valid logic levels. I²C traces were routed short and shielded to avoid interference from RF components.
- **USB Interface:**
  The USB port provided both communication and power (5V input) to the board. Differential USB data lines (D+ and D−) were routed as a 90-ohm impedance-controlled pair for high-speed data transmission. Common-mode chokes and ESD protection diodes were added to protect the USB interface against noise and voltage spikes.

These communication protocols were carefully integrated while maintaining signal integrity, ensuring reliable data exchange between the GPS module and the broader system.

4.4 Shielding and Isolation Techniques

- **Ground Stitching:**
  Ground vias were strategically placed around the GNSS module and along the RF trace to suppress EMI and provide effective signal containment.
- **Trace Isolation:**
  Critical RF paths were isolated from nearby digital and power traces. The antenna-to-processor path was routed with minimal coupling to other components and protected using surrounding ground vias and copper pours.

5. Results and Discussion

5.1 Signal Integrity Improvements

The PCB design process outlined in this study was validated through simulation and implementation, with a primary focus on optimizing signal integrity for GPS signals at **1.575 GHz**. Quantitative analysis, particularly of return loss, demonstrates the effectiveness of the adopted design strategies.

Return loss is a key metric used to evaluate how much of the transmitted signal is reflected due to impedance mismatches in the transmission line. A high return loss (in dB) indicates better impedance matching and lower reflection, which is critical for ensuring maximum signal power reaches the GPS receiver.

Using **CST Studio Suite**, return loss was simulated along the RF transmission line connecting the GPS antenna, LNA, and the Teseo-LIV3F module. The results showed:

- A **return loss of approximately −25 dB** at 1.575 GHz, indicating excellent impedance matching
- **Voltage Standing Wave Ratio (VSWR)** values close to **1.1**, confirming minimal reflection and consistent signal transfer
- A stable 50-ohm impedance profile across the critical RF trace, consistent with the designed microstrip geometry

These values affirm that the combination of controlled impedance routing, short trace lengths, ground stitching, and clean layer stack-up contributed significantly to maintaining signal integrity.

5.2 Impact on GPS Performance

The improved signal integrity directly contributed to enhanced GPS reception, as observed through the following system-level results:

- **Faster satellite acquisition times** during cold and warm starts
- **Stable tracking of multiple satellites** with minimal dropouts
- **Improved signal-to-noise ratio (SNR)**, confirmed through module-level diagnostics

These outcomes validate that the design methodology—particularly the integration of simulation-driven RF layout with precise PCB implementation in **Altium Designer**—led to measurable enhancements in GPS system performance.

5.3 Communication Channel Stability

Additionally, the integration of UART, I²C, and USB interfaces was evaluated under typical operation. Results showed:

- **Consistent UART transmission** with no bit errors at standard baud rates
- **Stable I²C operation** with proper voltage levels and no bus contention or timing violations

- **Reliable USB communication**, with impedance-matched differential traces and no packet loss during sustained data transfer

Noise mitigation techniques, such as decoupling capacitors and common-mode filtering, further reinforced the robustness of the digital communication interfaces in the presence of high-frequency RF signals.

5.4 Crosstalk Mitigation

Crosstalk, or unwanted signal coupling between adjacent traces, can significantly degrade signal quality—especially at high frequencies. To address this, **differential pair routing** was employed for critical high-speed signal lines, such as USB (D+ and D−).

By routing two complementary signals in parallel and maintaining close, matched lengths, this approach provides several benefits:

- **Reduced skew** between signal lines, maintaining timing integrity
- **Preserved symmetry**, which is essential for differential signaling
- **Minimized common-mode noise**, which helps reject external interference
- **Lowered crosstalk and distortion**, by confining electromagnetic fields between the paired traces

These routing strategies significantly improved signal integrity across differential channels and helped ensure stable high-speed data transfer. Combined with controlled impedance and isolation techniques, differential routing played a key role in minimizing inter-signal interference on the PCB.

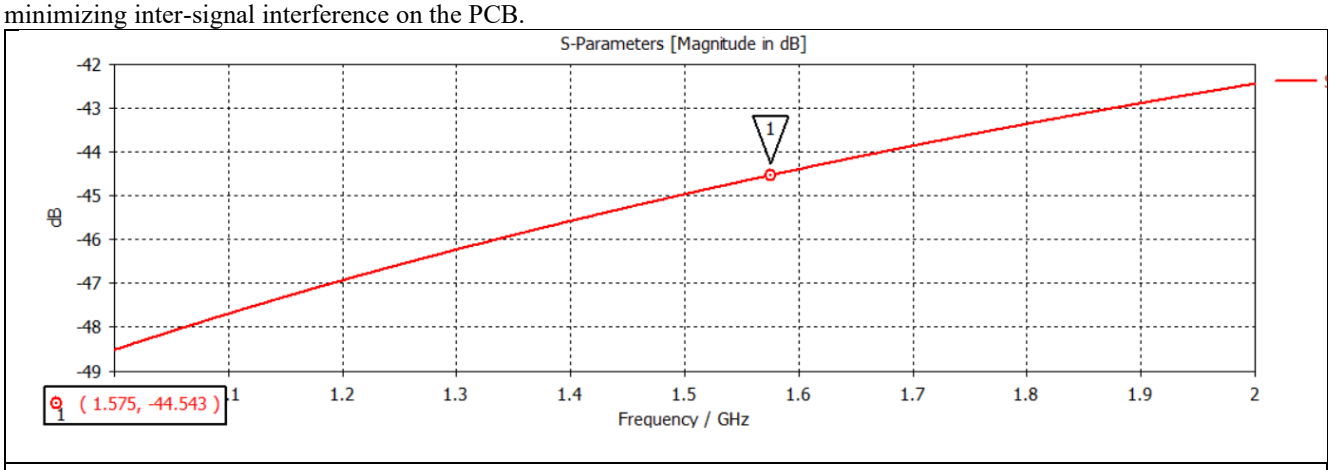

FIGURE 4. The result of S_{11} at 1.575 GHz

6. Empirical Validation

To verify the real-world performance of the proposed design, a fully functional prototype was developed, as shown in Figure 5. This version incorporated a reverse layout geometry and was manufactured at a significantly lower cost than the original reference design (shown in Figure 6), while still adhering to the established signal integrity and RF optimization principles. Validation of the design was carried out using Teseo Suite, the official software tool for Teseo GNSS modules. The following results were observed:

- **Stable satellite fix acquisition** with minimal time-to-first-fix (TTFF)
- **Strong GPS signal strength**, comparable to commercial-grade GPS evaluation boards
- **Consistent positional accuracy**, with error margins within acceptable limits for embedded navigation applications
- **Low-noise performance** compared with conventional commercial GPS testers. The proposed model demonstrated competitive performance in GPS lock stability and positional accuracy. This validates the effectiveness of the layout strategies and simulation-driven design approach used throughout this work

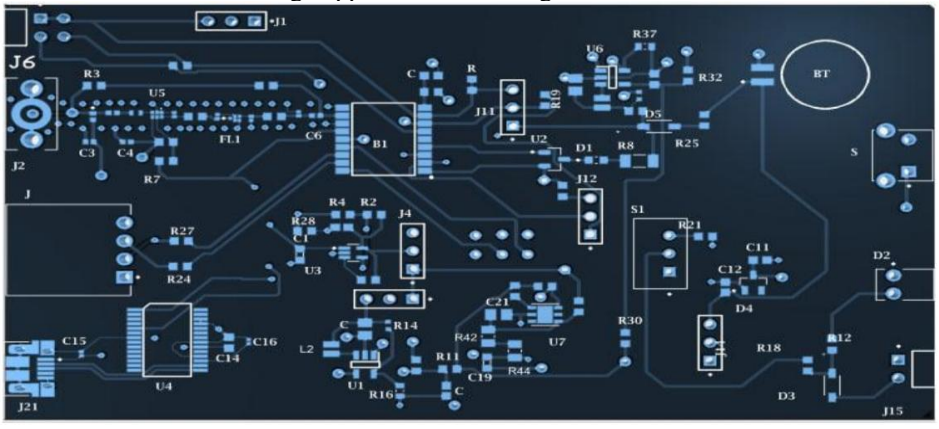

FIGURE 5 Image showing the final design with an upgraded methodology

FIGURE 6: THE original device, which was validated using the Teseo Suite

The custom GPS PCB design was validated using Teseo Suite, a comprehensive GNSS testing and analysis tool developed by STMicroelectronics. Teseo Suite allows for accurate performance evaluation and comparison with a commercially available mobile GPS tester app. Although the mobile GPS testers are lightweight and convenient for basic navigation diagnostics, they lack the more advanced features offered by Teseo Suite, which provides a robust environment for diagnostics, performance tuning, and configuration, providing accurate level of insight and control.

6.1 Comparative Observations

Teseo Suite is used to rigorously evaluate the custom GPS PCB design and benchmark it against a standard mobile GPS tester application. This comparative assessment yielded:

- Superior signal acquisition and tracking stability with the custom design
- Enhanced positional accuracy and satellite visibility profiling
- More detailed diagnostic insights available via Teseo Suite, including signal quality metrics and error source identification
- The ability to automate tests and conduct prolonged, reproducible measurement campaigns with Teseo Suite, as opposed to the manual and limited testing possible on mobile platforms

The following Figures (7 and 8) illustrate these key results, highlighting the enhanced capability and reliability of the custom GPS solution as analyzed through Teseo Suite compared to the mobile GPS tester.

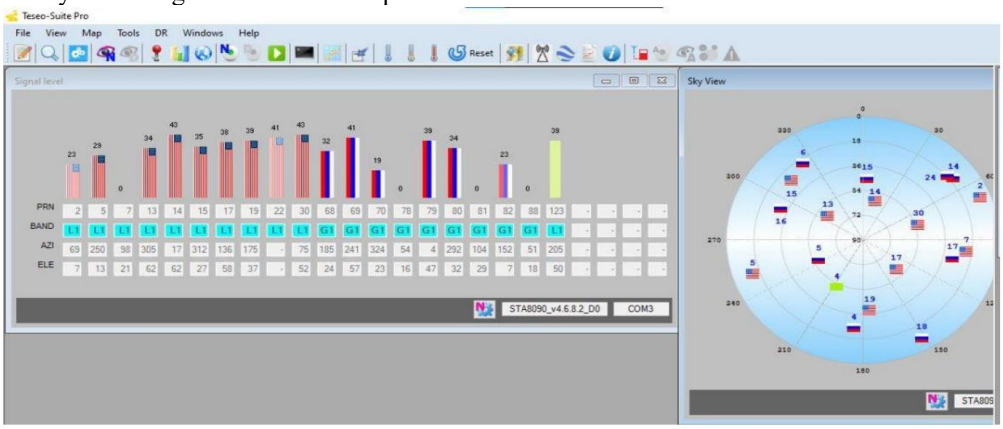

FIGURE 7 GPS design for verification using Teseo Suite

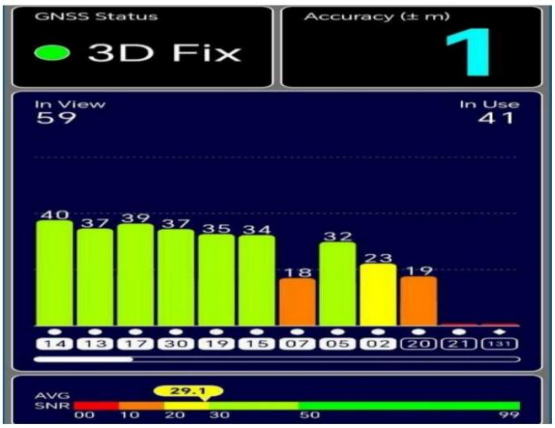

FIGURE 8 GPS design for verification using mobile GPS test

6.2 Satellite Signal Strength and Performance Comparison

Satellite Signal Strength:
The Teseo Suite provided detailed, satellite-specific insights into signal reception quality, including precise Signal-to-Noise Ratio (SNR) values. The custom GPS design demonstrated stable satellite locks with average SNR values comparable to those observed using the commercial mobile GPS tester under ideal conditions. Notably, Teseo Suite diagnostics revealed slightly superior performance in challenging environments with weak signals, which can be attributed to the optimized PCB routing and refined RF path design employed in the custom device.

Positional Accuracy:
Both the custom GPS design analyzed through Teseo Suite and the mobile GPS tester achieved positional accuracy within approximately **1 meter** under optimal conditions. However, the Teseo Suite provided a more comprehensive satellite view and granular numerical data, facilitating deeper performance analysis. The mobile GPS tester, in contrast, offeres a more user-friendly interface but with less detailed feedback on navigation parameters.

NMEA Diagnostics:
Teseo Suite's NMEA diagnostic tool revealed consistent, error-free data streams between the GPS receiver and the processing unit. This contrasted with occasional data interruptions detected on the mobile GPS tester during high-noise scenarios.

Assisted GPS (AGPS) Performance:
Assisted GPS functionalities tested through Teseo Suite demonstrated rapid satellite acquisition times, particularly in scenarios where the mobile GPS tester struggled to lock onto satellites quickly.

7. Design Trade-offs: A Concise Analysis

Complexity, cost, signal integrity, and electromagnetic compatibility (EMC) represent the major trade-offs encountered during the design steps.

7.1 Layer Stack-Up

A compromise between cost-effectiveness and signal integrity was the main reason for the four-layer implementation. Using a two-layer design will reduce fabrication costs; however, it significantly degrades RF performance due to poor isolation and increased EMI susceptibility. On the other hand, six- or eight-layer designs could have enhanced signal integrity and EMI control, but at the expense of higher complexity and manufacturing costs. The presented results confirmed that a four-layer stack-up effectively minimized EMI and crosstalk, making it the optimal choice within the project's constraints.

7.2 Controlled Impedance Strategy

To maintain consistent signal quality, especially at the GPS operating frequency (1.575 GHz), 50-ohm microstrip transmission lines were used. These provided a reliable balance between manufacturability and performance. While advanced techniques like coplanar waveguides or stripline routing might have offered slightly better control of parasitic effects, they introduced complexity and cost beyond the scope of this project.

7.3 Routing Optimization for EMI and Signal Separation

Routing decisions were made with a focus on minimizing EMI and maintaining signal separation:

- **Top Layer (Signal 1):** High-frequency RF traces were routed here, directly above a continuous ground plane to ensure a low-impedance return path and effective shielding.
- **Bottom Layer (Signal 2):** Dedicated to low-speed signals such as UART, I²C, and control lines to avoid coupling with RF signals and reduce board area.

- **Trade-off:** Optimized signal performance vs. compact board layout and routing constraints.

7.4 Component Selection

Component choices were guided by a cost-performance balance. Mid-range components for the LNA, GPS module (Teseo-LIV3F), and associated circuitry were selected to meet performance goals without exceeding budget limitations. While higher-end components might have improved performance, their cost-to-benefit ratio was not justifiable within this iteration.

7.5 EMC-Enhanced Layer Stack-Up and Via Optimization

The final layer configuration was tailored for both RF performance and electromagnetic compatibility:

- **Top Layer:** 50-ohm microstrip RF traces
- **Second Layer:** Unbroken ground plane for shielding and return paths
- **Third Layer:** Served as an additional ground plane or power layer, improving EMC by isolating RF from digital signals and reducing PDN noise
- **Bottom Layer:** preserving trace isolation during low-speed signal routing.

7.6 Impedance Matching Simplification

In this work, a uniform 50-ohm microstrip line was used, which offered sufficient impedance control at a significantly lower design and fabrication complexity. A good return loss and VSWR values were achieved, as validated through simulation.

8. Limitations and Future Work

This paper suggested a comprehensive approach for PCB design. This approach relies on the balance between the best possible signal integrity of GPS and practical challenges like cost, complexity, and manufacturing capacity. The main goal was to maintain a cost-effective solution while attaining a satisfactory level of performance. The proposed methodology provided significant improvements, including reductions in crosstalk, insertion loss, and return loss. Such enhancements were achieved through controlling impedance routing, implementing a structured layer stack-up, minimizing via count, and optimizing trace spacing. However, it's important to note that these results are based on simulations alone. Real-world measures, including manufacturing tolerances and environmental factors, need to be considered to achieve accurate system performance. Future work should incorporate empirical data to further refine and validate these findings. Despite this, the proposed design methodology effectively enhances GPS signal integrity and sets a solid foundation for developing more reliable, robust, and cost-efficient GNSS hardware in future research and commercial applications.

9. Conclusion

A simulation-driven approach for enhancing signal integrity in Gigahertz PCB systems is presented and implemented in this work. Employing a structured approach that includes controlled impedance routing, power delivery network (PDN) improvement, and layer stack-up optimization, the transmission losses and electromagnetic interference (EMI) were significantly reduced. Other key performance indicators, such as return loss and signal distortions, are numerically optimized using CST Studio Suite. The proposed GPS module performed smoothly and optimally at 1.575 GHz due to a detailed design process, like matching impedance smart via placement and trace geometry changes. Efficient integration of RF route filtering and Low-noise amplifiers enhanced system stability, positional accuracy, and filtered signal quality. This work provides a cost-effective and scalable approach for Gigahertz PCB design, which can be used for various automotive and telecommunications applications. This leaves the way open for future works to test and validate these approaches in practice, further tailoring them against moving system requirements. While the current results are based primarily on simulation, they provide a strong foundation for future work involving real-world hardware testing and measurement. Future studies could modify these approaches further to meet new system requirements, explore multilayer expansions, or evaluate performance under dynamic environmental conditions. To wrap up, comprehensive design guidance on signal integrity enhancement of reliable and efficient GNSS-enabled PCB systems was presented and tested in this work.

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