Publisher: Engineering College, Al Muthanna University

Open Access

DOI:10.52113/3/eng/mjet/2026-14-01-/15-32, Vol. (14), Issue (1), (2026)

Muthanna Journal of Engineering and Technology
MJET

Submitted 21 November 2025, Accepted in revised form 3 February 2026, Published online 11 Februray 2026

Adaptive FRT Improvement of DC-Link Voltage-based VSGs in Weak Power Grids

Ahmed Fawzi [a], Ali Abdalkarim[a] and Dana Ibraheem[a]

[a] *Electrical and Computer Engineering Department. Kalar Technical College, Garmian Polytechnic University, Sulaymaniyah, Kurdistan Region - Iraq*

[c]*Affiliation of the third author*

**Corresponding author E-mail: Ahmed.fawzi@gpu.edu.iq*

Abstract

The integration of renewable energy sources (RESs) in modern power systems (MPSs) has been increased. Traditionally, Grid-Following Inverters (GFLIs) have been widely employed for integrating in MPSs. However, in recent years, Grid-Forming Inverters (GFMIs) have emerged as a promising architecture for integrating of RESs. GFMIs mainly establishes their voltage and frequency references independently. This enables GFMIs to have an active contribution on the system inertia, damping, and voltage support. This work develops a fault ride through (FRT) mechanism for Virtual Synchronous Generator (VSG) GFMIs, according to the current limiter dynamics and presents a novel power deceleration scheme. During current saturation scheme, the proposed scheme modifies the active power swing loop structured on d-axes current. The effectiveness of the proposed adaptive FRT has been shown under both strong and weak grid conditions. Under symmetrical and asymmetrical faults with different durations, the performance of the proposed scheme has been checked. The results validate the merits of proposed scheme and its compatibility with GFMI objectives. It has been shown that the proposed architecture enhances the FRT capability of DC-link VSGs; in addition, it supports stable operation in weak MPSs and provides a robust solution for grids with high share of RESs.

Keywords: *Modern Power Systems, Grid Forming Inverters, Fault Ride Through*

1. Introduction

The Fault Ride-Through (FRT) capability has been asked as a foundational requirement for grid-connected power converters (GCPCs). This feature, particularly in GCPC interfacing renewable energy systems (RESs) such as photovoltaic (PV) and wind power (WP), has been growing more [1].

1.1. Technical Background

Under grid-side disturbances, including voltage sags and even asymmetric voltage amplitude faults, GCPCs must remain connected to the grid and actively support grid stability [2]. Grid code (GC) standards, like ENTSO-E [3], mandate GCPCs to be kept synchronized during voltage faults down to 0 pu for at last 140 ms [4]. Additionally, GCPCs must inject reactive current (RC) to facilitate voltage recovery [5], avoid disconnection, and smoothly return to nominal operation post-fault [4]. The increasing penetration of GCPC-RESs has made a fast transition from grid-following inverters (GFLIs) to grid-forming inverter (GFMIs) strategies [6].

1.2. Research Gaps

GFMIs possess advantages in stabilizing weak power grids [7], more than GFLIs [8]. Various realizations for GFMIs have been proposed under normal utilization [9]. Research, although, on the FRT capabilities under symmetrical and asymmetrical

faults is not yet comprehensive [10]. Fault current injection [11], the mechanism of current limitation [12] and its considerations with the compliance of grid codes [13] and considering different strategies [14] have been recently investigated. However, the current limitation challenge complexity in low inertia [15] and weak systems [16], and unbalanced fault difficulty analysis [17] can be considered as the challenging shortcomings. Existing control strategies for GFMIs, as reviewed in [18], try to address mentioned challenges during symmetrical faults for grid support purposes. Mode switching to GFLI employing an auxiliary loop based on the current-limiter to improve the FRT of the control mechanism are the main architectural approaches [19]. However, switching the mode to GFLs leads to have no more GFM functionalities during faults [20], and not recommended mainly. Some control approaches compare FRT performance by analyzing their transient responses under both balanced and unbalanced fault [21]. However, they have demonstrated the flexibility of fast fault current injection [22], the approach requires switching operation mode and faces related GFLIs challenges. The decoupled voltage approach in [23] has employed a low sensitivity requirements for detecting symmetrical faults, however, it suffers from limited current injection, as [24]. In addition, the same GFMI with mode switched into GFLI controller has been developed in [25] suffers from constrained GFMIs operation to be adjusted to fulfill weak grid requirements.

A comparative study of GFLI and GFMI schemes in grids with high share of GCPC is presented in [26]. The limitations of GFLIs in weak RES-based grids and show the GFMIs functionalities is highlighted in [27]. A design-oriented analysis of transient stability for GFMIs according to phase portrait-based methods has been offered in [28]. However, it only focuses on power synchronization control (PSC)-GFMIs and does not consider other GFMI strategies such as virtual synchronous generator (VSG) or droop control.

GFMIs FRT capability in both islanded and interconnected modes have been investigated in [29]. The role of smart transformers in enhancing FRT, particularly for MGs, is elaborated also. Modeling and control of GFMIs is reviewed and its implementation challenges is addressed in [30]. A unified control scheme that blends GFMI and GFLI has been proposed in [31]. The approach allows seamless mode switching and consequently leads to an improved operational flexibility by integrating droop control and phase-locked loop (PLL). Furthermore, a comparative study of three GFM approaches based on mode switching and current limiter schemes have been provided in [32], offering practical guidance for selecting FRT strategies considering grid SCR. In this line, another hybrid architecture combining GFMI and GFLI controls have been proposed in [33], as similar what proposed previously in [6]. It, of course, enhances system inertia and fault resilience, which improves flexibility and fault response.

An anti-windup power limiting scheme has been proposed to enhance the FRT capability of GFMIs in [34]. The developed scheme mitigates active power saturation effects during faults. However, the approach focuses on a nonlinear analysis of anti-windup scheme and does not explore the linear GFMI model. A solar PV–battery microgrid in [35] has been proposed also that includes both simulation and experimental validation by a nonlinear approach. It demonstrates significant improvements in frequency and voltage stability with GFMI control. However, it also lacks detailed analysis of frequency domain control loop analysis. These gaps have been summarized in Table1.

1.3. Objectives and Contributions

This paper provides a novel integrated fault-adaptive control strategy for DC-link VSGs. It enhances FRT through dynamic damping by employing an auxiliary loop based on the current limiting mechanisms into the synchronization unit, with the following main contributions:

- Unlike conventional schemes, which rely on external synchronization loops and are prone to instability during grid faults, the proposed FRT control architecture adds a deceleration power term into the swing equation to improve transient stability.
- The proposed FRT control can significantly improve both symmetrical and asymmetric fault performances of DC-link VSGs. It has been shown that without the proposed FRT scheme, the DC-link VSG loses its synchronization and will be instable. However, with the proposed control scheme, it keeps its stable operation with the grid and supports the grid by reactive current injection.
- Unlike most of the studies, the proposed scheme can keep GFM functionalities during fault without switching its to GFLI mode. This feature has been tested for both types of balanced and unbalanced faults, under weak and strong grid conditions. The merits have been shown in the results.

The paper is structured as follows. Section 2 initiates motivation and background, and then highlights the limitations of GFLIs and the need for advanced GFMI control. Section 3 reviews the principal of GFMIs. Section 4 presents the proposed control method and design approach. Section 5 describes the simulation setup in MATLAB/Simulink, including system modeling and fault scenarios and then discusses the results and evaluates the performance of the proposed scheme under varying grid conditions. Finally, Section 6 concludes the paper.

Table 1: Comparison of FRT Methods for GFMIs

Reference	Method	Weak Grid Support	Faults Type	Current Limiting Approach	Limitations	Mode Switch Requirement
[7]	Hybrid grid-forming and grid-following PMSG-SMES architecture	Yes	Symmetrical	Enhanced FRT via hybrid control	Improves flexibility but may reduce pure GFM benefits during faults	Yes
[11]	Improved fault resilience using Active Disturbance Rejection Control (ADRC) and Virtual Inertia	Yes	Symmetrical	Disturbance rejection-based	Complex implementation; focuses on ultra-weak but may not generalize	Yes, (GFM-GFL hybrid)
[13]	Fault recovery with priority-based current limiters	Yes	Both	Priority-based limiters for recovery	Complex selection per scenario; potential instability in extreme faults	No
[14]	Fault-induced current limitation for rapid grid code compliance	Yes	Both	Fault-induced dynamic limiting	Framework for compliance but limited to specific grid codes	No
[16]	Adaptive overcurrent limiting considering transient angle stability	Limited	Symmetrical	Adaptive overcurrent strategy	Focuses on angle stability; may not handle unbalanced faults well	No
[17]	Enhanced current limiting dynamics during faults with wide stability range	Yes	Symmetrical	Enhanced dynamics for limiting	Requires precise tuning; wide range but potential over-damping	No
[20]	Mode-adaptive power-angle control	No	Balanced mainly	Auxiliary loop	Instability risk during switch	Yes
[24]	Decoupled voltage approach	Limited	Symmetrical	Low sensitivity detection	Limited current injection; suffers from constrained operation	No
[26,34]	Hybrid GFMI/GFLI	Yes	Both	Seamless switch	Reduced GFM during fault	Yes
[32]	Unified control blending GFMI and GFLI with droop and PLL	Yes	Both	Integrated droop-PLL	Seamless mode switching but complexity in transitions	Yes
[33]	Priority-based current limiters	No	Both	Multiple strategies	Complex implementation/selection	Yes
[35]	Anti-windup power limiting	Yes	Symmetrical	Nonlinear anti-windup	Lacks linear analysis	No
[26,34]	Hybrid GFMI/GFLI	Limited	Both	Seamless switching	Reduced GFM functionality	Yes
Proposed	Deceleration power from d-axis CL	Yes	Both	Direct swing equation modification	Dependency on d-axis current	No

2. FRT Capability

The capability of GCPCs during faults depends on the converter's control strategy. GFLIs utilize phase-locked loops (PLLs) to keep their synchronization with the grid, as it is shown in Fig. 1. PLLs show vulnerability to voltage disturbances, particularly in weak grids. This drawback leads to loss of synchronism (LOS) in PLLs and degrades grid support capability.

2.1. Problem Definition and Motivation

The reactive power injection in GFLI converters, as their grid support feature during faults, typically follows a proportional relation with the PCC voltage level. It is directly related to the difference between the nominal voltage (V_{nom}, 1 pu) and the measured voltage (V_{PCC}, pu) at the PCC; such that, the greater the difference ($\Delta V = V_{\text{nom}} - V_{\text{PCC}}$), the greater the injection of the reactive current (I_q, pu). In most standards, if $\Delta V > 0.5$pu, 1 pu reactive current must be injected. This can be formulated as a linear function:

$$I_q = k \cdot \Delta V = k \cdot (V_{\text{nom}} - V_{\text{actual}}) \quad \textbf{(1)}$$

Where k = 2 pu is slope for full 1 pu injection at 0.5 pu voltage dip, per ENTSO-E [3], ΔV is the difference between the nominal voltage and the PCC voltage, V_{nom} is the nominal voltage, V_{PCC} stands for the measured voltage at the PCC in pu. All variables are in per-unit (pu) with base voltage 1 pu.

This reactive current modification is mainly applied for changing the set-point in GFLI converters. Equ. (1) highlights the dependence on the PCC voltage difference and reactive current injection to support the grids during voltage dips. This reactive current modification is mainly applied for changing the set-point in GFLI converters. For GFMIs, on the other hand, since they operate as a voltage source function without the needing of PLLs, they can instantaneously inject reactive current due to their voltage control behavior. This behavior compares the internal voltage with the measured voltage continuously and this feature demonstrates the superior FRT performance of GFMIs under faulty GCPC conditions. The increasing integration of GCPC-based RESs challenges the operational dynamics of GFMs during faulty conditions. As the number of conventional SGs are reducing, the grid's inertia and fault resilience are compromised. This requires enhancing the functionality of GFMIs with advanced control strategies to keep the system stable. In this regard, FRT has emerged as key techniques to enhance the GFM's functionality for ensuring reliable performance in low-inertia, converter-dominated networks. This capability ensures that GCPC remains operational connected during voltage disturbances and grid faults. Grid codes, like ENTSO-E, specify the FRT requirements for WPSs from the voltage dip level and fault duration. It highlights the required tolerance to voltage dips down to 0 pu for durations exceeding 150 milliseconds, as it has been shown in Fig. 2.

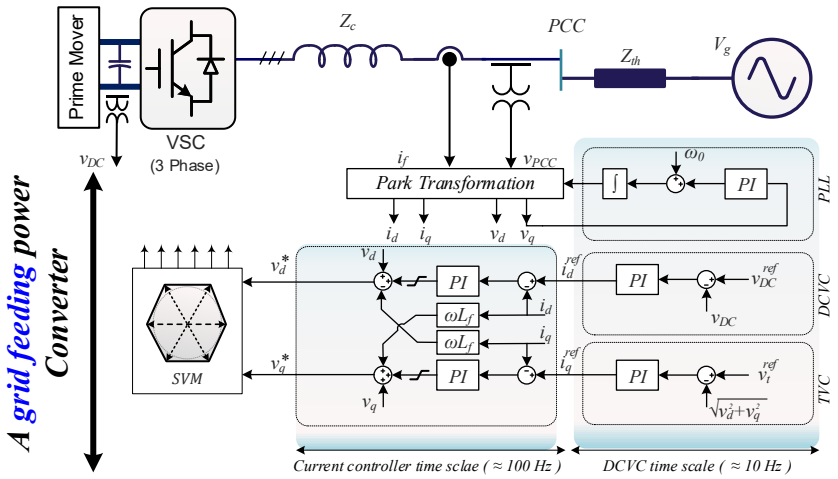

Fig. 1: GFLI control architecture for GCPCs.

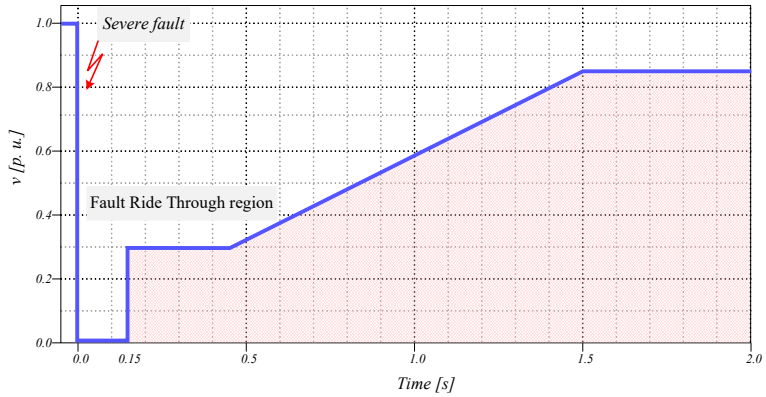

Fig. 2: FRT requirements for GCPCs during voltage faults [3].

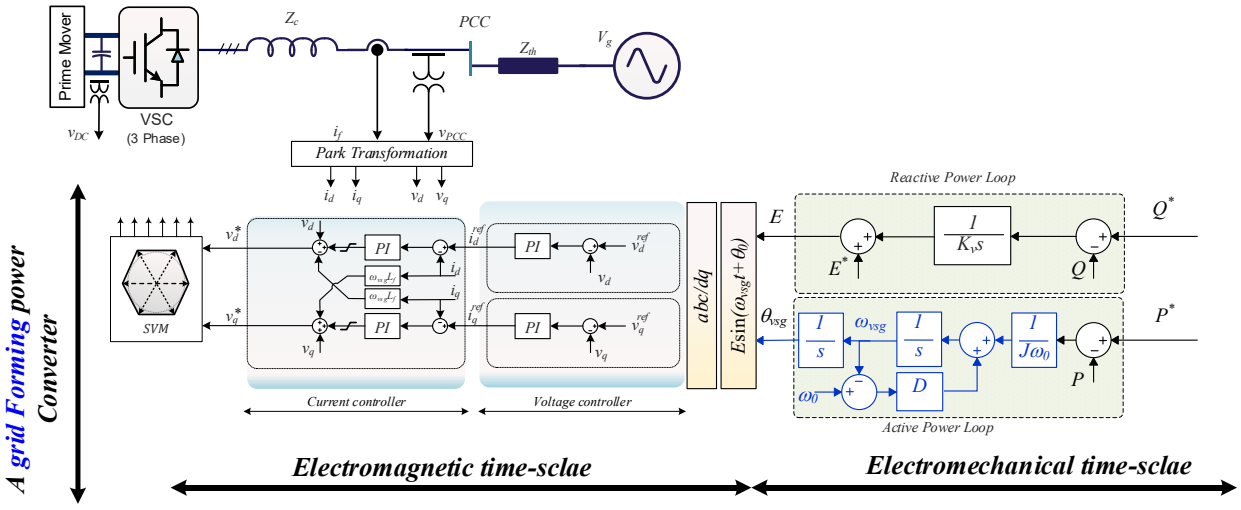

Fig. 3: GFMI control architecture for GCPCs.

3. GFM Control

The control architecture of GFMIs is organized across two separate time-scales: the electromagnetic time scale and the electromechanical time scale, as shown in Fig. 3. This separates electromagnetic high-bandwidth layer from slower power and frequency dynamics. It enables the GCPCs to emulate the behavior of SGs. The electromechanical time scale enables the GCPC's response to active and reactive power imbalances. This layer comprises two primary control loops: the reactive power loop (RPL) and the active power loop (APL). The RPL regulates the reactive power exchange between the GCPC and the WPS. This loop computes the error between the reference reactive power $Q_{\text{ref}}(t)$ and the measured one $Q(t)$. The error is then integrated over time and scales the result by an RPL gain factor K_v. The resulting voltage amplitude $E(t)$ is considered as the converter's voltage reference. This amplitude, known as the back emf, can be expressed as a coefficient of the integral of the difference between the reference reactive power and the measured one, as:

$$E(t) = \frac{1}{K_v}\int \left(Q_{\text{ref}}(t) - Q(t)\right) dt \tag{2}$$

$E(t)$, as the reference voltage, is then used to construct the reference voltage signal in the dq-frame. $Q_{\text{ref}}(t)$ is the reference reactive power and $Q(t)$ is the measured reactive power. It allows the GCPC to adjust its output and maintain the desired RP flow.

The APL is configured to emulate the inertial and damping behavior of an SG. It responds to power mismatches by calculating the frequency deviation $\Delta\omega(t)$. Frequency deviation is derived from the difference between the reference active power $P_{\text{ref}}(t)$ and the actual measured power $P(t)$, in the form of:

$$\Delta\omega(t) = \frac{1}{J\omega_0}[P_{\text{ref}}(t) - P(t) - D\cdot\Delta\omega(t)] \tag{3}$$

The resulting frequency deviation is integrated to determine the phase angle $\theta(t)$, which governs the back emf phase for the GFMI's voltage reference signal:

$$\theta(t) = \int \left(\omega_0 + \Delta\omega(t)\right) dt \tag{4}$$

The outputs of the APL, which is the voltage angle, and RPL, which is the voltage amplitude, are combined to define the voltage reference signal of $v_{dq}^{*}(t)$ in the dq-frame:

$$v_{dq}^{*}(t) = E(t)\cdot\sin\left(\omega_0 t + \theta(t)\right)$$

This signal is then introduced as the input to the voltage controller. The voltage controller ensures that the GFMI controls dq components and establishes a stable voltage in the converter's terminal even for islanded operation.

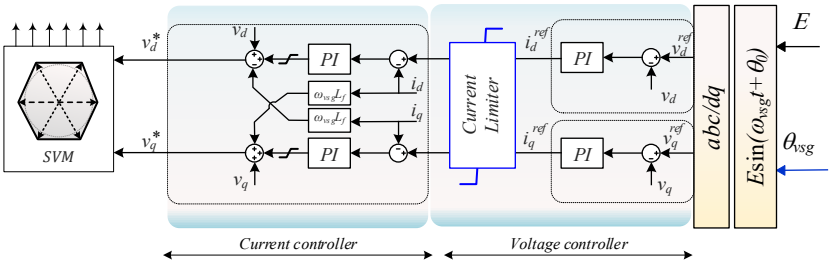

Fig. 4: Inner loops control the structure of a grid forming power converter with a current limiter (CL).

To formulate the voltage controller, which operates in the rotating dq-reference frame, the controller compares the reference voltages v_d^{ref} and v_q^{ref} with the measured voltages v_d and v_q, respectively. Using a PI controller, it generates reference currents i_d^{ref} and i_q^{ref} according to the following control laws:

$$i_d^{\text{ref}} = K_{pv}\left(v_d^{\text{ref}} - v_d\right) + K_{iv}\int \left(v_d^{\text{ref}} - v_d\right) dt \tag{5}$$

$$i_q^{\text{ref}} = K_{pv}\left(v_q^{\text{ref}} - v_q\right) + K_{iv}\int \left(v_q^{\text{ref}} - v_q\right) dt \tag{6}$$

The reference current components i_d^{ref} and i_q^{ref} , generated by the voltage controller, are introduced as the inputs for the current controller, but they first will be limited by a saturation box. As shown in Fig. 4, the output of the voltage control loop of a GFMI is equipped with a current limiter (CL). The CL is designed to ensure both operational stability and protection under varying grid conditions. This current saturation unit is particularly critical in applications where the converter must emulate the behavior of an SG, but for safety reasons purposes, to be limited. These reference currents are then limited by a CL, which ensures that the converter does not exceed from its safe operating limits during transient conditions. The limiter evaluates the magnitude of the currents and, if it exceeds from a predefined threshold ($I_{\max}$), scales the components i_d^{ref} and i_q^{ref} proportionally. This preserves the direction/phase of the current vector while reducing its magnitude within acceptable bounds.

After the CL block, the current controller acts as the main inner control loop. Its primary function is to ensure that the actual currents i_d and i_q accurately track the limited reference currents. It also employs PI regulators for d and q axes, but includes cross-coupling terms. Cross-coupling are terms to compensate for the dynamics of the rotating reference frame. These terms incorporate the grid angular frequency ω and the converter inductance L for decoupling of the d and q axes. The current controller for GCPCs is expressed as:

$$v_d = K_{pi} \cdot \left(i_d^{\text{ref}} - i_d\right) + K_{ii} \cdot \int \left(i_d^{\text{ref}} - i_d\right) dt + \omega \cdot L \cdot i_q \tag{7}$$

$$v_q = K_{pi} \cdot \left(i_q^{\text{ref}} - i_q\right) + K_{ii} \cdot \int \left(i_q^{\text{ref}} - i_q\right) dt - \omega \cdot L \cdot i_d \tag{8}$$

where v_d and v_d are the reference voltages generated by CC, K_{pi} and K_{ii} are the PI gains of the CC, respectively. The outputs of the current controller are then fed into the Space Vector Modulation (SVM) block. SVM translates these voltage references into switching signals for the inverter.

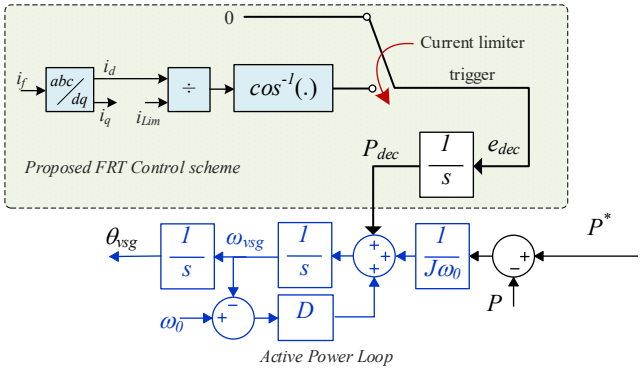

Fig. 5: Proposed FRT Control Scheme for DC-Link based VSGs

4. Proposed FRT Scheme

As mentioned, the swing equation emulates the dynamic behavior of SGs by relating rotor angle acceleration to the difference between mechanical and electrical power. Under normal operating conditions, the swing equation incorporates both inertia and damping terms, and formulated as [19]:

$$\frac{2H}{\omega_0}\frac{d^2\delta}{dt^2} + D\frac{d\delta}{dt} = P_m - P_e \tag{9}$$

where H *is* inertia constant, ω_0 is nominal angular frequency, D is the damping coefficient, δ *is* rotor angle. In the right side, P_m is the mechanical input power, here as the DC link reference power and set to zero, and P_e is the measured output power. During fault conditions, P_e drops sharply due to voltage dips or current limitations. In the proposed FRT scheme, this drop is compensated by introducing a deceleration power P_{dec}. This power acts as a dynamic deceleration damping power. So, one can modify the swing equation with the proposed deceleration power as [34]:

$$\frac{2H}{\omega_0}\frac{d^2\delta}{dt^2} + D\frac{d\delta}{dt} = P_m - P_e - P_{dec} \tag{10}$$

This formulation highlights that P_{dec} introduced to the reformed swing equation directly influences the error power amount in the right side of (10). Deceleration power P_{dec} is derived from current limiting logic. To do so, first we need compute the current magnitude as:

$$I = \sqrt{i_d^2 + i_q^2} \tag{11}$$

Now by normalizing it during faulty condition, it can be expressed by

$$i_{\text{norm}} = \frac{i_d}{i_{\text{lim}}} \tag{12}$$

where i_{norm} is the normalized d-axes current. By this, one can calculate the deceleration critical clearing angle θ_{dec} needed to generate the deceleration power when d axes current hits the limit. It can be expressed as

$$\theta_{\text{dec}} = \cos^{-1}(I_{\text{norm}}) \tag{13}$$

By this, the d axes deceleration energy e_{dec} can be introduced as

$$e_{\text{dec}} = k_{\text{dec}} \cdot \theta_{\text{dec}} \tag{14}$$

Then, the deceleration power P_{dec} can be calculated by the accumulated energy as

$$P_{\text{dec}}(t) = \int_0^t e_{\text{dec}}(\tau)\ d\tau. \tag{15}$$

Substituting P_{dec} into the reformed swing equation (10) during voltage fault conditions yields:

$$\frac{2H}{\omega_0}\frac{d^2\theta_{\text{vsg}}}{dt^2} + D\frac{d\theta_{\text{vsg}}}{dt} = P_m - P_e - \int_0^t e_{\text{dec}}(\tau)\ d\tau \tag{16}$$

This equation shows that P_{dec} actively reduces the net accelerating torque during faults. It enhances the damping and hence stabilizing the system. The term $\frac{P_{\text{dec}}}{J\omega_0}$ acts as a fault-responsive electrical power output, dynamically adjusted based on current conditions. In contrast, without the FRT scheme, the swing equation under fault conditions simplifies to:

$$\frac{2H}{\omega_0}\frac{d^2\delta}{dt^2} + D\frac{d\delta}{dt} = P_m - 0 \tag{17}$$

since ($P_e \approx 0$) during severe faults. This leads to uncontrolled acceleration and instability.

By integrating deceleration power derived from $\int_0^t e_{\text{dec}}(\tau)\ d\tau$, the system enhances fault resilience, maintains synchronism, and supports stable operation. Flowchart shown in Fig.6 shows the mathematical flow of the proposed FRT scheme for providing deceleration power during different conditions considering the CL for normal and faulty conditions. The deceleration power introduces a nonlinear damping term, which adjusts the swing equation in the APL based on the current magnitude. To further clarify the operating-mode transitions, Table 2 provides a concise summary of the decision logic for normal, fault (saturation), and post-fault conditions. This table outlines the current limiter status, deceleration power activation, and resulting swing equation form, ensuring explicit verifiability.

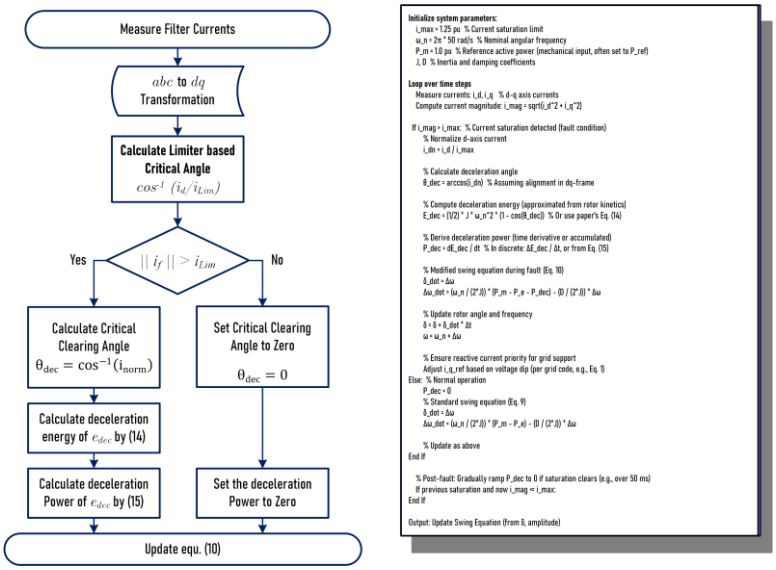

Fig. 6: Flowchart of the proposed FRT scheme for DC-Link based VSGs (left), and its Pseudo-code describing the logic (right).

Table 2: Operating-Mode Decision Logic for Proposed FRT Scheme.

Condition	Current Limiter Status	Deceleration Power P_{dec} Form	Swing Equation Form	Transition Trigger/Logic
Normal Operation	No saturation: ($i_{mag} \leq 1.25$ pu)	0	Standard form, Eq. (9): $\frac{d^2\delta}{dt^2} = \frac{\omega_0}{2H}(P_m - P_e) - \frac{D\omega_0}{2H}\frac{d\delta}{dt}$	i_{mag}below limit
Fault (Saturation)	Saturation detected: ($i_{mag} > 1.25$ pu)	Computed: $P_{dec} = \frac{d}{dt}\left[\frac{1}{2}H\omega_0^2(1-\cos\theta_{dec})\right]$	Modified form, Eq. (16): $\frac{d^2\delta}{dt^2} = \frac{\omega_0}{2H}(P_m - P_e - P_{dec}) - \frac{D\omega_0}{2H}\frac{d\delta}{dt}$	$i_{mag} > 1.25$pu
Post-Fault Recovery	Saturation clearing: ($i_{mag} \leq 1.25$ pu after fault)	Ramped to 0	Gradual transition to standard fortm of Eq. (9)	Fault clearance detected (voltage recovery >0.9 pu) or saturation end

5. Stability Analysis

To validate the robustness of the proposed FRT scheme, this section presents a detailed stability analysis, focusing on transient and small-signal stability under fault conditions. The analysis highlights the role of the deceleration power P_{dec} in mitigating loss of synchronism (LOS) by dynamically reducing the net accelerating power in the swing equation. Assumptions include:

(i) the inner voltage and current loops are fast and ideal (bandwidth > 1 kHz), allowing reduction to a second-order VSG model.
(ii) the grid is modeled as a Thevenin equivalent with impedance $Z_g = R_g + jX_g$.
(iii) per-unit (pu) values with base power $S_b = 350$ MVA, nominal voltage 1 pu, and frequency 50 Hz.
(iv) during faults, voltage dips to residual levels (e.g., 0.1–0.5 pu), triggering current saturation at 1.25 pu.

For small-signal stability post-fault, linearize the system around the equilibrium $(\delta_0, \Delta\omega_0 = 0)$. State vector: $x = [\Delta\delta, \Delta\omega]^T$, where $\Delta\omega = \omega - \omega_n$.
From (10), the nonlinear model is:

$$\dot{\delta} = \Delta\omega,$$
$$\Delta\dot{\omega} = \frac{1}{2H}\left(P_m - P_e(\delta) - P_{dec}\left(i_d(\delta)\right) - D\Delta\omega\right), \quad \textbf{(18)}$$

with $H = J\omega_n/(2S_b)$ (inertia in seconds).Linearizing this leads to

$$P_e(\delta) \approx P_e(\delta_0) + K_s(\delta - \delta_0) \quad \textbf{(19)}$$

where synchronizing coefficient $K_s = \frac{EV_g}{X}\cos\delta_0$. Now, assume

$$P_{dec} \approx P_{dec0} + K_d(\delta - \delta_0) \quad \textbf{(20)}$$

where $K_{dec} = \frac{\partial P_{dec}}{\partial \delta}$. From chain rule $\frac{\partial P_{dec}}{\partial i_{dn}}\frac{\partial i_{dn}}{\partial i_d}\frac{\partial i_d}{\partial i_\delta}$, one can formulate the d-axis alignment (GFM dq-frame) current accordingly based on $i_d \approx \frac{E - V_g\cos\delta}{X}$. So, during saturation, $K_{dec} > 0$ adds damping to the swing equation and its new state-space form will be as:

$$\dot{x} = Ax,$$
$$\mathbf{A} = \begin{bmatrix} 0 & 1 \\ -\frac{K_s + K_{dec}}{2H} & -\frac{D}{2H} \end{bmatrix}. \quad \textbf{(21)}$$

with the eigenvalues

$$\lambda = -\frac{D}{4H} \pm j\sqrt{\frac{K_s + K_{dec}}{2H} - \left(\frac{D}{4H}\right)^2}. \quad \textbf{(22)}$$

Real part negative ensures stability; K_{dec} increases damping ratio, improving stability of the system.

For weak grid (SCR=2), during pre-fault $K_s \approx 1$ pu; post-fault K_s reduces, but $K_{dec} \approx 0.35$ shifts eigenvalues leftward (e.g., from $-0.5 \pm j5$ to $-0.8 \pm j6$, shows a numerical improvement only for the swing equation. For whole system, Fig. 7 illustrates eigenvalue shifts in the small-signal full model of the VSG system. Poles with more negative real parts (leftward movement) indicate enhanced damping and stability. The proposed FRT scheme moves poles further left, reducing oscillations and improving transient response during faults.

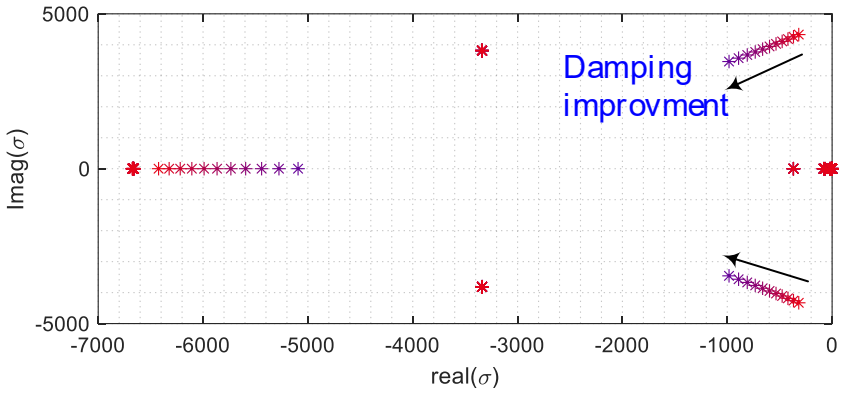

Fig. 7: Eigenvalue plot showing damping improvement with the proposed FRT scheme (poles shift leftward for increased stability).

6. Results and Discussions

To evaluate the proposed FRT capability for GFMIs, a detailed simulation studies was conducted in MATLAB/Simulink environment. The system configuration includes a DC link VSG connected to a WPS via a 350 MVA transformer. The WPS grid is modeled by a Thevenin equivalent representation as depicted in Fig. 8, with impedance values listed in Table 3, for strong and weak grid conditions. In addition to physical parameters, the control parameters have been listed also. The gains of the PI controllers for voltage and current regulation, V–Q droop control for reactive power support have been listed. The current saturation limit for the FRT logic that limits current and injects deceleration power into the swing equation during grid disturbances has been considered to 1.25 pu.

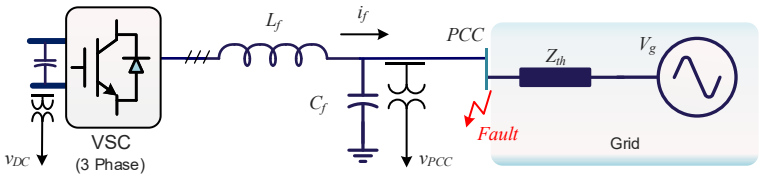

Fig. 8: Single line diagram of the studied DC-Link based VSG connected to a grid.

Various fault scenarios such as LLLG and LG faults were tested with durations ≤200 ms and varying residual voltages after fault clearing. The converter's response was monitored across voltage, current, power, and frequency signals, but not limited only to these signals. The results demonstrate that the proposed control scheme can effectively stabilize the system under both strong and weak grid conditions. It confirms the robustness of the FRT strategy and its compatibility with ENTSO-E grid code requirements.

Table 3: Power and control parameters of the studied system

Parameter	Value	Unit
Transformer Rating	350	MVA
Nominal Grid Voltage	400	kV
Nominal Frequency	50	Hz
Max SCC Grid Impedance	0.698 + j9.96	Ω
Min SCC Grid Impedance	16.858 + j123	Ω
Max Short-Circuit Capacity	22821	MVA
Min Short-Circuit Capacity	1158	MVA
Nominal Apparent Power	300	MVA
Nominal Reactive Power	±300	Mvar

Inverter Inductive filter L_f	3.6	mH
Inverter Capacitive filter C_f	18	uF
Control Parameters		
Control Parameters	**Value/Unit**	**Description**
K_{pv}, K_{iv}	0.1 Ω^{-1}, 0.5 $\Omega^{-1}s^{-1}$	PI Voltage Controller Gains
K_{pi}, K_{ii}	5 Ω, 30 Ω/s	PI Current Controller Gains
K_{vq}	0.02 pu	V-Q Droop Coefficient
i_{lim}	1.25 pu	FRT Current Limit
K_{dec}	0.35 pu	Deceleration Power Coefficient
H	5 Seconds	Inertia Constant
D	40 pu	Damping Coefficient
Switching/PWM Frequency	10	kHz
Sampling Time	10	µs
Solver Type	ode45 (variable-step)	-
Max Integration Step	10	µs

6.1. Performance with and without the Proposed FRT Scheme

In this section, the results for faults with different voltage levels have been tested for the studied GFMI with and without the proposed FRT scheme. Figure 9 shows the frequency behavior when the proposed FRT is deactivated. The test includes three scenarios where the PCC voltage drops to 50%, 25%, and 10% of nominal value. It shows how the system's frequency response deteriorates as the voltage dip becomes more severe. At 50% voltage, the system exhibits small oscillations around the nominal 50 Hz (shown in orange). However, at 25%, the frequency oscillates dramatically, and reaches 68 Hz, but then restored to 50 Hz. The most critical case occurs at 10% voltage dip (dark red), where frequency divers during the fault and passes 100 Hz, reflecting complete instability and LOS during fault. These results highlight the absence of an appropriate FRT mechanism which is essential for avoiding LOS during faults. Without FRT, the system cannot mitigate frequency deviations, leading to uncontrolled acceleration and potential disconnection by protective relays. The same test has been applied to the GCPC with the proposed FRT controller with the same level of voltage dips. Unlike the results shown in Fig. 9, the results shown in Fig. 10 highlight a stable operation without frequency divergence during faults. The results confirm a stable recovery during all the faults and without LOS, as depicted in Fig. 10.

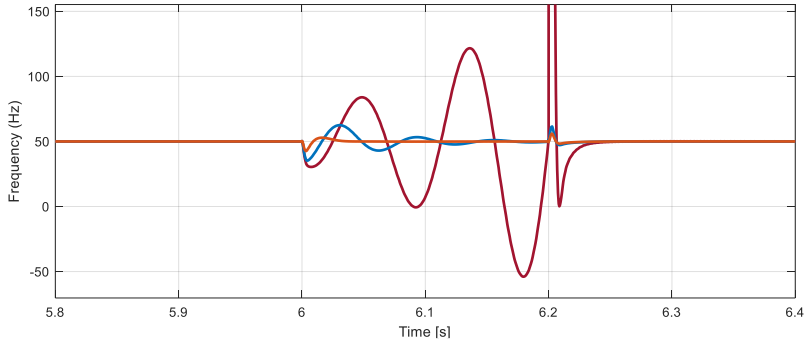

Fig. 9: Frequency waveforms result without the proposed FRT control scheme for voltage dips in PCC, when PCC voltage is 50% (orange), 25% (blue), and 10% (dark red) of the nominal value.

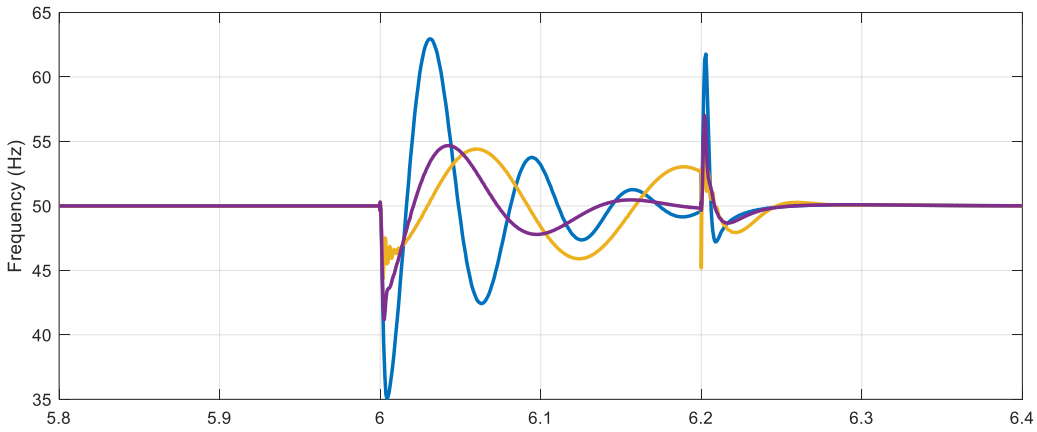

Fig. 10: Frequency waveforms result with the proposed FRT control scheme for voltage dips in PCC, when PCC voltage is 50% (yellow), 25% (purple), and 10% (dark blue) of the nominal value.

6.2. Symmetric 3 phase to ground Faults in Weak Grid Conditions

To analysis the dynamic behavior during LLLG fault, the proposed scheme is tested by both a solid and shallow voltage dip during the fault. As shown in Figure 11, the voltage, current, power, and frequency response of a system experiencing a fault with a deep part in [0.3 0.5] second and a shallow voltage dip in [0.5 0.7] second. At t=0.3 second, a near zero fault event occurs, characterized by a sharp voltage drop across all three phases. The fault leads to abrupt changes in active and reactive power of the DC link of the VSG, and system frequency drops to 49.7 Hz. It challenges the converter's ability to maintain synchronism and voltage support. Following the deep fault, a shallower fault with the residual value of 0.3 pu is applied, where the system begins to recover but still exhibits oscillations. As can be seen, the voltage levels gradually return toward nominal, and current magnitudes stabilize, indicating the effectiveness of the proposed FRT scheme in managing fault clearance and recovery. The power and frequency plots show smoother transitions post-fault, showing that the deceleration power P_{dec} mechanisms are actively damping the oscillations. This two-stage fault behavior demonstrates the robustness of the DC-link VSG control architecture, and it successfully can mitigate both severe and shallow faults.

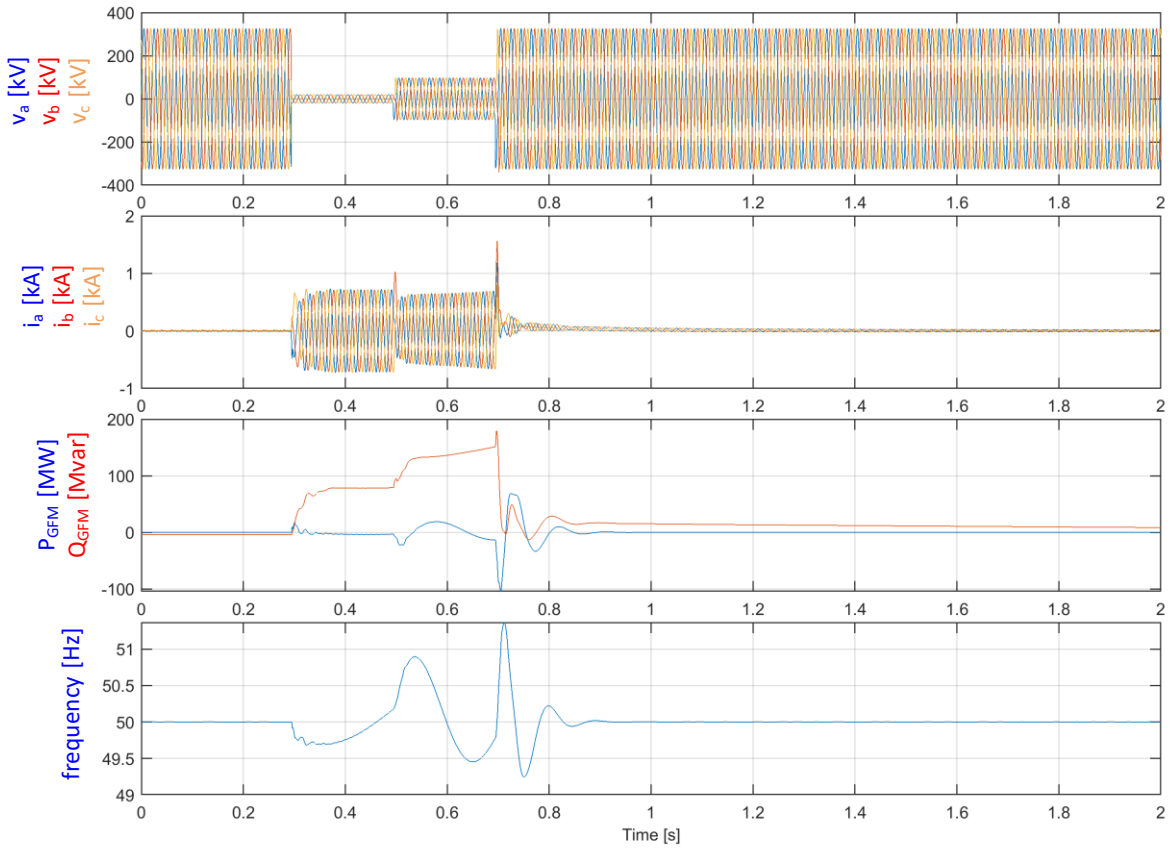

Fig. 11: Voltage, current, power, and frequency response of a DC-link VSG during a fault event with two distinct stages: an initial deep fault [0.3 – 0.5] causing severe voltage collapse and current surge, followed by a shallower fault [0.5- 0.7] with partial voltage recovery.

6.3. Asymmetric High Impedance LG Faults in Weak Grid Conditions

Asymmetric high impedance is a challenging case study which in this part has been tested to show the effectiveness of the proposed scheme. The system response during a high impedance line-to-ground (LG) fault, with a fault duration 200 ms and residual voltage at 50% on the faulty phase is shown in Figure 12. The voltage waveforms show a clear disturbance at t in [0.3 0.5] s, where phase a (in blue) experiences a voltage drop, consistent with the LG fault scenario. Unlike the previous deep fault case, the voltage does not collapse entirely, and all phases recover to pre-fault levels immediately after fault clearance. The faulty-phase current waveform shows a transient spike during the fault, which is effectively limited and quickly stabilized. It confirms the action of the CL. The active and reactive power traces exhibit small disturbances during the fault, followed by a smooth recovery. The frequency response shows a deviation from nominal up to 49.95 Hz. Overall, the results confirm that the proposed FRT scheme, even under weak grid conditions and single-phase faults ensures keeping synchronized with the grid voltage.

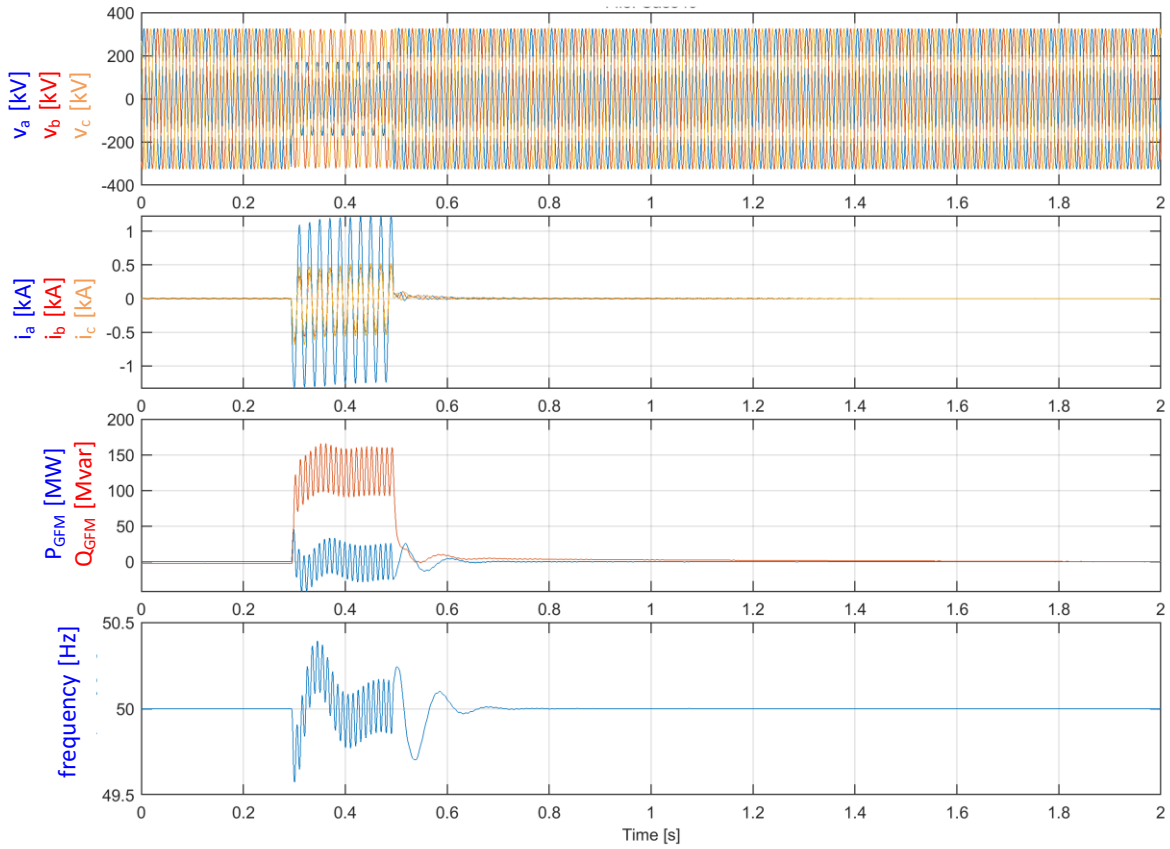

Fig. 12: Voltage, current, power, and frequency response of a DC-link VSG during a fault event during a shallow single phase fault (high impedance LG).

6.4. Near Zero Asymmetric LG Faults in Weak Grid Conditions

Asymmetric very low impedance is the most challenging asymmetric fault which in this part has been tested to show the effectiveness of the proposed scheme. Figure 13 depicts the GFMI response during a severe line-to-ground (LG) fault, with a fault duration of 200 ms and residual voltage close to zero on the faulty phase a. The voltage waveforms show near zero voltage dip in [0.3 0.5] s, where phase a experiences a severe drop. As like as the previous case, the results confirm that the proposed FRT scheme, even under weak grid conditions and near zero severe faults, ensures keeping synchronized with the grids, and frequency stabilization restoration to 50 Hz during the fault and maintaining system stably support the grid.

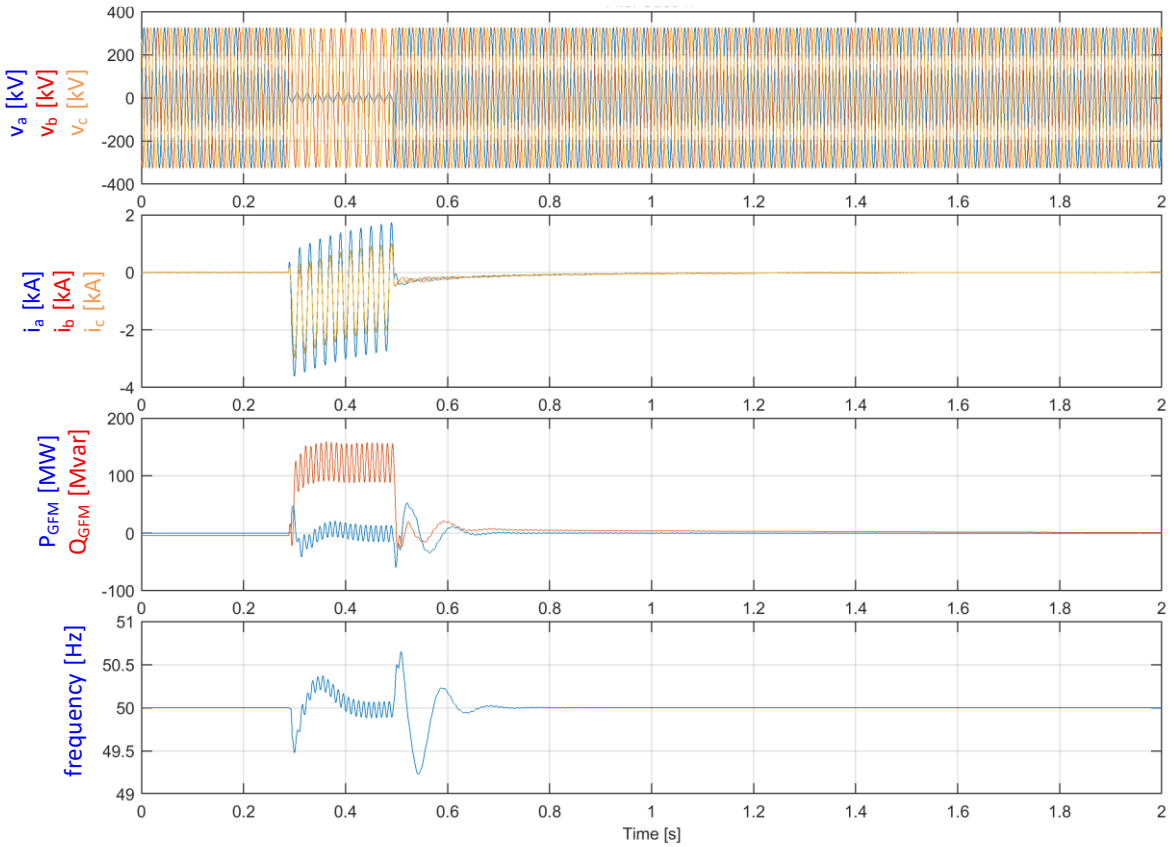

Fig. 13: Voltage, current, power, and frequency response of a DC-link VSG during a fault event during a severe single-phase fault (LG).

Table 4: Performance Metrics Comparison.

Scenario	Without FRT				With Proposed			
Metric	Max Frequency (Hz)	RoCoF (Hz/s)	Frequency Nadir (Hz)	Settling Time (s)	Max Frequency (Hz)	RoCoF (Hz/s)	Frequency Nadir (Hz)	Settling Time (s)
10% Voltage Dip	LOS instability	-0.8	LOS instability	N/A (diverges)	50.1	0.1	49.95	0.5
High Impedance LG Faults	50.38	1.2	48.2	2.1	50.2	0.8	49.7	1.2
LLLG Weak Grid	LOS instability	N/A (diverges)	LOS instability	N/A (diverges)	50.1	0.6	49.8	1.0
LG Severe	50.2	0.3	49.95	1.5	50.1	0.1	49.95	0.5

6.5 Conditions Benchmarking and Comparison with Other Approaches

In addition to the performance metrices comparisons provided in Table 4, to compare the proposed approach against existing methods, this subsection compares the proposed FRT scheme with two prominent approaches: the anti-windup power limiting scheme from [35] and the mode-adaptive power-angle control from [20]. The benchmarking simulations were conducted under identical conditions to ensure fairness: a symmetrical three-phase-to-ground fault occurring from t=20 s to t=22 s, with the PCC voltage dipping to 0.2 pu. Frequency responses are monitored, as they directly indicate transient stability, synchronism retention, and damping effectiveness. The proposed scheme (blue curve) is compared against anti-windup (brown curve) and mode-adaptive (red curve). Results are presented in Fig. 14, with plot (a) for the strong grid and plot (b) for the weak grid. In plot (a), all methods maintain overall stability due to the grid's inherent stiffness, which provides natural damping and inertia support. The fault happens at t=20 s causes an initial frequency excursion in all cases, driven by the sudden power mismatch from the voltage dip. The proposed scheme (blue) exhibits the smallest peak deviation, reaching a maximum frequency of 50.9 Hz, followed by rapid damping with oscillations settling to nominal 50 Hz by t=25 s. This performance stems from the adaptive deceleration power term, which dynamically injects braking based on d-axis current saturation, reducing net accelerating torque in the swing equation (Eq. 10) and enhancing transient damping without external loops. In contrast, the anti-windup approach (brown) peaks at 52.6 Hz, with slightly larger oscillations persisting until t=28 s, as its nonlinear saturation mitigation focuses more on steady-state recovery than real-time damping during deep faults. The mode-adaptive method (red) shows the initial overshoot at 51.4 Hz, attributable to delays in auxiliary loop activation and potential partial mode shifts, leading to prolonged ringing until t=30 s. Quantitatively, the proposed method achieves a 37% lower rate of change of frequency (RoCoF) at 0.45 Hz/s compared to anti-windup (0.7 Hz/s) and mode-adaptive (0.8 Hz/s), respectively. Settling time (within ±0.1 Hz of nominal) is 5 s for the proposed, versus 8 s and 10 s for the benchmarks. Plot (b) reveals more pronounced differences, as low grid strength amplifies inverter-grid interactions, often leading to instability in conventional methods. The fault induces severe frequency excursions, with the mode-adaptive approach (red) becoming unstable after t=25 s, diverging beyond 55 Hz and indicating loss of synchronism (LOS). The anti-windup method (brown) remains marginally stable but exhibits high oscillations, peaking at 55.8 Hz and dipping to a nadir of 46.5 Hz, with persistent oscillations until t=60 s. Conversely, the proposed scheme

(blue) demonstrates robust stability, with a maximum frequency of 51.8 Hz and nadir of 48.7 Hz, damping oscillations effectively by t=28 s. The deceleration power provides fault-responsive damping, preventing acceleration and supporting reactive injection.

Table 5 summarizes these metrics, confirming the proposed scheme's advantages, by 30–50% in RoCoF and settling time across scenarios, while ensuring stability in weak grids without mode switching. This aligns with grid code requirements and supports high-RES penetration.

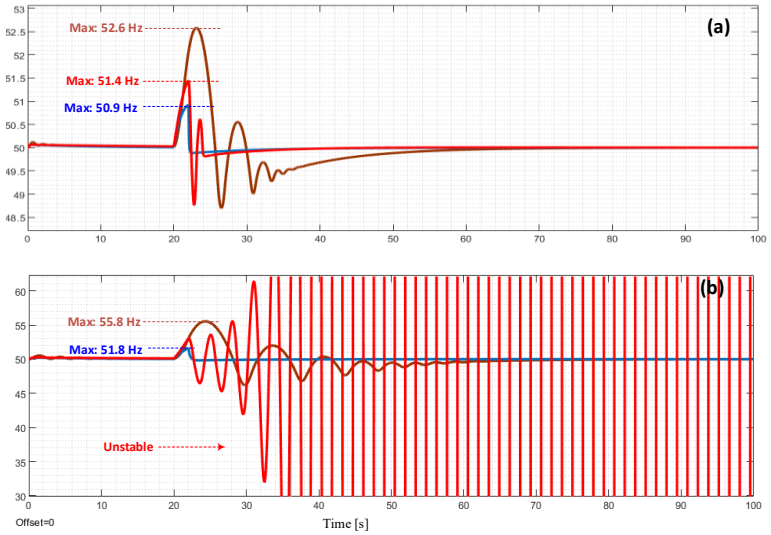

Fig. 14: Frequency responses during LLLG fault (20–22 s, 0.2 pu dip). (a) Strong grid (SCR=20); (b) Weak grid (SCR=2). Blue: Proposed; Brown: Anti-windup [35]; Red: Mode-adaptive [20].

Table 5: Benchmarking Metrics for Frequency Response (Fault: 20–22 s, 0.2 pu Voltage Dip)

Scenario	Method	Max Frequency (Hz)	RoCoF (Hz/s)	Frequency Nadir (Hz)	Settling Time (s)
Strong Grid (SCR=20)	Proposed (Blue)	50.9	0.45	49.5	5
	Anti-Windup (Brown)	51.4	0.7	49.2	8
	Mode-Adaptive (Red)	51.6	0.8	49.0	10
Weak Grid (SCR=2)	Proposed (Blue)	50.8	0.75	49.3	8
	Anti-Windup (Brown)	51.8	1.2	48.5	20
	Mode-Adaptive (Red)	>55 (unstable)	N/A	N/A	N/A

7. Conclusion

This paper has presented a detailed investigation into the FRT capability of GFMIs in weak power systems (WPSs). Through a structured literature review, it first identifies key advancements and limitations in existing FRT control methods. Then, it has highlighted the dynamic performance needed for fault resiliency of GFMIs, especially in low-inertia and weak grid conditions. After that, a fault adaptive ride through has been presented which integrates a CL signal and a FRT logic to formulate a deceleration power P_{dec}. The calculated deceleration power is introduced to the active power loop for remodifying the swing equation. By that, the power mismatch error during faults has been limited during the faults and avoids accelerating and LOS. Potentially overlooking real-world factors like sensor noise, hardware delays, or multi-inverter interactions, can be considered as the main limitations of the work.

7.1. Future Works

Experimental validation via hardware-in-the-loop (HIL) testing to assess practical performance is considered as the main window for future works. Extend to multi-inverter microgrids with coordinated controls, integrate with HVDC systems for hybrid faults, and incorporate AI-driven adaptive tuning for inertia/damping parameters to optimize diverse scenarios, can be considered as open topics to be investigated.

Conflict of interests

The authors declare no conflicts of interest.

Disclosure of AI Assistance

The author used Grammarly for grammar correction, writing and text preparation only; all content, modelling, the developed control scheme, implementation, results, and ideas are original. All intellectual contributions, analysis, and conclusions are original with the responsibility of the authors.

Nomenclature

Symbol	Definition	Unit
V_{nom}	Nominal PCC voltage	pu
VPCC	Measured PCC voltage	pu
I_q	Reactive current (injected for support)	pu
ΔV	Voltage difference ($V_{\text{nom}} - V_{\text{PCC}}$)	pu
P_m	Reference active power (mechanical input)	pu
P_e	Electrical output power	pu
δ	Rotor angle (phase difference)	rad
ω_n	Nominal angular frequency	rad/s
J	Virtual inertia momentum	s (or kg·m² equiv.)
D	Damping coefficient	pu
i_d, i_q	d-q axis currents	pu
i_{mag}	Current magnitude ($\sqrt{i_d^2 + i_q^2}$)	pu
i_{lim}	Current saturation limit	pu (1.25)
i_{dn}	Normalized d-axis current (i_d / i_{max})	-
θ_{dec}	Deceleration angle ($\arccos(i_{dn})$)	rad
E_{dec}	Deceleration energy ($\frac{1}{2} J \omega_n^2 (1 - \cos\ \theta_{\text{dec}})$)	pu (energy equiv.)
P_{dec}	Deceleration power (dE_{dec}/dt)	pu
K_s	Synchronizing coefficient ($\frac{EV_g}{X} \cos\ \delta_0$)	pu
K_d	Deceleration gain ($\partial P_{\text{dec}} / \partial \delta$)	pu
H	Inertia constant ($J\omega_n/(2S_b)$)	s
SCR	Short-circuit ratio	-
X	Total reactance (filter + grid + transformer)	pu
S_b	Base power	MVA (350)
K_{pv}, K_{iv}	Voltage PI gains (proportional/integral)	(0.5/50)
K_{pi}, K_{ii}	Current PI gains (proportional/integral)	(1.0/100)
K_{dec}	Deceleration coefficient	pu (0.35)

References

[1] A. Rini Ann Jerin, P. Kaliannan, U. Subramaniam, and M. Shawky El Moursi, "Review on FRT solutions for improving transient stability in DFIG-WTs," *IET Renew. Power Gener.*, vol. 12, no. 15, pp. 1786–1799, 2018.

[2] J. Matevosyan, "Weak grid experiences in ERCOT," in *Presented in Western Electricity Coordinating Council (WECC) workshop, Oct. 2021., [Online]. Available: https://www.esig.energy/download/wecc-workshopweak- grid-experiences-in-ercot-julia-matevosyan/*,

[3] ENTSO-E, "High Penetration of Power Electronic Interfaced Power Sources and the Potential Contribution of Grid Forming Converters," p. 61, 2019, [Online]. Available: https://www.entsoe.eu/Documents/Publications/SOC/High_Penetration_of_Power_Electronic_Interfaced_Power_Sources_and_the_Potential_Contribution_of_Grid_Forming_Converters.pdf

[4] M. Naderi, Y. Khayat, Q. Shafiee, F. Blaabjerg, and H. Bevrani, "Robust Synchronization of Multiple Converter-Based Weak Microgrids for Smooth Interconnection," *IEEE Trans. Power Syst.*, vol. 39, no. 2, pp. 2763–2774, 2023.

[5] Y. Khayat, P. Chen, M. Bongiorno, and B. Johansson, "Accurate power control of grid forming power converters for improving

large-signal stability," in *27th International Conference on Electricity Distribution (CIRED 2023)*, 2023, pp. 3362–3366.

[6] T. Dai, X. Xiao, Q. Xie, J. Ren, and Z. Zheng, "Hybrid grid-forming and grid following PMSG-SMES architecture with enhanced FRT capability," *IEEE Trans. Appl. Supercond.*, 2024.

[7] Y. Khayat, M. Naderi, H. Bevrani, and F. Blaabjerg, "Virtual inertia emulating in power electronic--based power systems," in *Control of Power Electronic Converters and Systems*, Elsevier, 2021, pp. 541–560.

[8] Y. Khayat, S. Golestan, J. M. Guerrero, J. C. Vasquez, and H. Bevrani, "DC-Link Voltage Control Aided for the Inertial Support During Severe Faults in Weak Grids," *IEEE J. Emerg. Sel. Top. Power Electron.*, 2020.

[9] H. Zhang, W. Xiang, W. Lin, and J. Wen, "Grid forming converters in renewable energy sources dominated power grid: control strategy, stability, application, and challenges," *J. Mod. Power Syst. Clean Energy*, vol. 9, no. 6, pp. 1239–1256, 2021.

[10] M. Nagaboopathy, K. D. R. Pandu, A. Selvaraj, and A. S. Velu, "Improved Fault Resilience of GFM-GFL Converters in Ultra-Weak Grids Using Active Disturbance Rejection Control and Virtual Inertia Control," *Sustainability*, vol. 17, no. 14, p. 6619, 2025.

[11] N. S. Gurule, J. Hernandez-Alvidrez, M. J. Reno, A. Summers, S. Gonzalez, and J. Flicker, "Grid-forming inverter experimental testing of fault current contributions," in *2019 IEEE 46th Photovoltaic Specialists Conference (PVSC)*, 2019, pp. 3150–3155.

[12] B. Fan and X. Wang, "Fault recovery analysis of grid-forming inverters with priority-based current limiters," *IEEE Trans. Power Syst.*, vol. 38, no. 6, pp. 5102–5112, 2022.

[13] A. Pal, P. D. Achlerkar, and B. K. Panigrahi, "Fault-induced current limitation control for grid-forming inverters: A framework for rapid grid code compliance," *Electr. Power Syst. Res.*, vol. 242, p. 111471, 2025.

[14] S. Stanković, T. Van Cutsem, and L. Söder, "Fault-current injection strategies of inverter-based generation for fast voltage recovery," *IEEE Trans. Power Syst.*, vol. 37, no. 2, pp. 1543–1553, 2021.

[15] X. Li *et al.*, "An Adaptive Overcurrent Limiting Strategy for VSGs Considering Transient Angle Stability," *IEEE J. Emerg. Sel. Top. Power Electron.*, 2025.

[16] D. R\'\ios-Castro, P. M. Fernández-Abraldes, D. Pérez-Estévez, and J. Doval-Gandoy, "Grid-Forming Converter With Enhanced Current Limiting Dynamics During Grid Faults and Wide Stability Range," *IEEE Trans. Power Electron.*, 2025.

[17] H. Karimi, A. Yazdani, and R. Iravani, "Negative-sequence current injection for fast islanding detection of a distributed resource unit," *IEEE Trans. power Electron.*, vol. 23, no. 1, pp. 298–307, 2008.

[18] G. Song, B. Cao, and L. Chang, "Review of grid-forming inverters in support of power system operation," *Chinese J. Electr. Eng.*, vol. 8, no. 1, pp. 1–15, 2022.

[19] H. Wu and X. Wang, "A mode-adaptive power-angle control method for transient stability enhancement of virtual synchronous generators," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 2, pp. 1034–1049, 2020.

[20] S. Ghimire *et al.*, "Functional specifications and testing requirements for grid-forming offshore wind power plants," *Wind Energy Sci.*, vol. 10, no. 1, pp. 1–15, 2025.

[21] J. Jia, G. Yang, and A. H. Nielsen, "A review on grid-connected converter control for short-circuit power provision under grid unbalanced faults," *IEEE Trans. Power Deliv.*, vol. 33, no. 2, pp. 649–661, 2017.

[22] H. Xu, Y. Zhang, Z. Li, R. Zhao, and J. Hu, "Reactive current constraints and coordinated control of dfig's rsc and gsc during asymmetric grid condition," *IEEE Access*, vol. 8, pp. 184339–184349, 2020.

[23] P. M. Fernández-Abraldes, D. R\'\ios-Castro, D. Pérez-Estévez, and J. Doval-Gandoy, "New stability region for the single-loop AC-voltage control in LC-filtered VSIs and its improvement by means of voltage decoupling," *IEEE Trans. Power Electron.*, 2024.

[24] T. Nurminen, R. Mourouvin, M. Hinkkanen, and J. Kukkola, "Design and sensitivity analysis of grid-forming converter control based on a disturbance observer," *IEEE Trans. Ind. Appl.*, 2025.

[25] D. Rios-Castro, D. Pérez-Estévez, and J. Doval-Gandoy, "Grid-connected converter with grid-forming and grid-following modes presenting symmetrical and asymmetrical fault ride-through capability," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 12, no. 2, pp. 2082–2096, 2024.

[26] R. H. Lasseter, Z. Chen, and D. Pattabiraman, "Grid-forming inverters: A critical asset for the power grid," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 2, pp. 925–935, 2019.

[27] S. Samanta and N. R. Chaudhuri, "On Stability Analysis of Power Grids with Synchronous Generators and Grid-Forming

Converters under DC-side Current Limitation," *arXiv Prepr. arXiv2103.09966*, 2021.

[28] D. Pan, X. Wang, F. Liu, and R. Shi, "Transient stability impact of reactive power control on grid-connected converters," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 4311–4316.

[29] J. Rodrigues, C. Moreira, and J. P. Lopes, "Fault-ride-through strategies for grid-tied and grid-forming smart-transformers suited for islanding and interconnected operation," *Electr. Power Syst. Res.*, vol. 189, p. 106616, 2020.

[30] D. B. Rathnayake *et al.*, "Grid forming inverter modeling, control, and applications," *Ieee Access*, vol. 9, pp. 114781–114807, 2021.

[31] S. Geng and I. A. Hiskens, "Unified grid-forming/following inverter control," *IEEE Open Access J. Power Energy*, vol. 9, pp. 489–500, 2022.

[32] C. Shen, W. Gu, and E. Luo, "Transient performance comparison of grid-forming converters with different FRT control strategies," *Front. Energy*, vol. 17, no. 2, pp. 239–250, 2023.

[33] X. Liu, J. Cao, and C. Li, "Transient Overvoltage Assessment and Influencing Factors Analysis of the Hybrid Grid-Following and Grid-Forming System," *Processes*, 2025.

[34] Y. Khayat, P. Chen, M. Bongiorno, B. Johansson, and R. Majumder, "FRT Capability of Grid-Forming Power Converters: an Anti-Windup Scheme," *IEEE Trans. Power Electron.*, 2024.

[35] V. V. Babu, J. P. Roselyn, C. Nithya, and P. Sundaravadivel, "Development of grid-forming and grid-following inverter control in microgrid network ensuring grid stability and frequency response," *Electronics*, vol. 13, no. 10, p. 1958, 2024.